[

]. CX-1597C

]. *Id.* [

]. *See id.*

c. Claim 3

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 3.

i. The method according to claim 2,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 2.

ii. wherein said first pattern is a predetermined pattern unique from all possible representations of said fourth pattern.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 3, "wherein said first pattern is a predetermined pattern unique from all possible representations of said fourth pattern."

[

CX-1597C CX-0559C

CX-1597C

CX-0559C

]. CX-1597C

CX-0559C

See CX-1597C

]. *See id.*

d. Claim 4

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 4.

i. The method according to claim 2,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 2.

ii. wherein said fourth pattern comprises (i) between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 4, "wherein said fourth pattern comprises (i) between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state."

[

CX-1597C

].

[

]. *Id.*

e. Claim 5

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 5.

i. The method according to claim 4,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 4.

ii. wherein said second bit follows said first bits.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 5, "wherein said second bit follows said first bits."

[

].

See CX-1597C (Reinman WS) at Q&A 271. [

]. *See id.* at Q&A 272.

f. Claim 6

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 6.

i. The method according to claim 1,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 1.

ii. wherein said first pattern comprises a plurality of bits each having a first state.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 6, "wherein said first pattern comprises a plurality of bits each having a first state."

[

]. *See* CX-1597C (Reinman WS) at Q&A 270. [

]. *See id.* at Q&A 273.

g. Claim 7

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 7.

i. The method according to claim 1,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 1.

ii. wherein said second pattern comprises between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 7, "wherein said second pattern comprises between zero and a plurality of first bits having a first state and (ii) a second bit having a second state opposite said first state."

[CX-0559C

CX-0559C

]" *See* CX-1597C

]. *See id.*

[

]. *See id.*

h. Claim 8

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 8.

i. The method according to claim 1,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 1.

ii. wherein said third pattern comprises a binary number.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 8, "wherein said third pattern comprises a binary number."

[

]. *See* CX-1597C [

]. *Id.*

[

]. *Id.*

i. Claim 9

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 9.

i. The method according to claim 1,

As shown above, the MediaTek decoders do not satisfy all limitations of claim 1.

ii. wherein said codeword in compatible with at least one of an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264.

The evidence shows that the MediaTek decoders satisfy the additional limitation of claim 9, "wherein said codeword in compatible with at least one of an International Organization for Standardization/International Electrotechnical Commission 14496-10 standard and an International Telecommunication Union-Telecommunications Standardization Sector Recommendation H.264."

[

]." CX-1597C

See CX-0642

CX-

; CX-1597C].

[

].

CX-1597C (Reinman WS) at Q&A 276.

j. Claim 11

The record evidence shows that the MediaTek decoders do not satisfy all limitations of claim 11.

i. A system comprising:

The MediaTek [ ] used in the accused Funai H.264 products are each a system. CX-1597C (Reinman WS) at Q&A 276.

ii. a decoder configured to generate a codeword; and

The evidence shows that [ ] decoders each satisfy the limitation of "a decoder configured to generate a codeword." [ ] each include a decoder configured to generate a codeword. CX-1597C (Reinman WS) Q&A 277.

[

JX-0019C ; CX-0642

; CX-1597C].

iii. [ ]

[

CX-1597C

]. *See id.*

iv. **(i) set an index value to a threshold in response to a first portion of said codeword having a first pattern,**

For the reasons discussed above with respect to step (A) of claim 1, the evidence does not show that the MediaTek decoders satisfy this claim limitation.

v. **(ii) add an offset to said index value based on a second pattern in a second portion of said codeword following said first portion in response to said first portion having said first pattern and**

For the reasons discussed above with respect to step (B) of claim 1, the evidence does not show that the MediaTek decoders satisfy this claim limitation.

vi. **(iii) add a value to said index value based on a third pattern in a third portion of said codeword following said second portion in response to said first portion having said first pattern.**

For the reasons discussed above with respect to step (C) of claim 1, the evidence does not show that the MediaTek decoders satisfy this claim limitation.

4. Indirect Infringement

Complainants allege that Funai is liable for induced infringement and contributory infringement of claims 1-9 of the '663 patent. Compls. Br. at 277-82. As discussed above, Complainants have not established direct infringement of these claims. Nevertheless, the record evidence does establish that Funai would be liable for both induced infringement and contributory infringement of claims 1-9, in the event it is determined that there is direct infringement of these claims.[38]

a. Induced Infringement

The evidence shows that Funai markets the accused Funai H.264 products to U.S. consumers by featuring the accused H.264 high-definition playback functionality. *See* CX-1597C (Reinman WS) at Q&A 290. For example, the leaflet for [ ] states that "It is fully future proof as it supports 1080p signals from all sources, including the most recent like Blu-ray and advanced HD game consoles." *See* CX-0609 ([ ]) at 2. In addition, the same leaflet advertises H.264 as a playback format. *Id.* at 3. As another example, the leaflet for [ ] lists features such as "Blu-ray Disc playback." *See* CX-0124 ([ ]) at 1; CX-1597C (Reinman WS) at Q&A 290.

In addition, Funai creates and distributes product manuals for the accused Funai H.264 products that provide instructions regarding how to set-up and operate the products, including instructions that describe how to use the accused processes to play back H.264-compliant HD video. CX-1597C (Reinman WS) at Q&A 291. For example, the user manual for the

[38] The GR12 Filing indicates that this Initial Determination should address the issue of whether Funai indirectly infringes claim 11 of the '663 patent, but Complainants did not brief this issue. *See* GR12 Filing at 7; Compls. Br. at 277-82. Accordingly, the administrative law judge declines to make findings with respect to whether Funai indirectly infringes claim 11 of the '663 patent.

[ ] provides instructions on how to watch H.264-encoded and other MPEG videos using DLNA. *Id.*; CX-0046 ([ ]) at 15-16. In addition, the user manual for [ ] provides instructions on how to "use your Blue-ray disc/DVD player," which necessarily includes accused processes for UEGk decoding high-definition H.264-encoded Blu-ray discs. CX-0056 ([ ]) at 10; CX-1597C (Reinman WS) at Q&A 291. There are more such examples throughout the product literature for the accused Funai H.264 products. CX-1597C (Reinman WS) at Q&A 291 (listing specific product literature examples).

Moreover, the evidence shows that Funai provides, or arranges for the provision of, technical support to ensure that end users are able to operate all features of the accused Funai products in the United States, including the accused H.264-compliant high-definition video playback features. CX-1597C (Reinman WS) at Q&A 292. This technical support is made available through a website accessible in the United States, as well as through a U.S. Customer Support Line. *Id.* For example, the user manual for the [ ] states: "For further assistance, call the customer support service in your country." CX-0609 ([ ]) at 1. In addition, the manual states: "If you cannot resolve your problem, refer to the FAQ for this [ ]." *Id.* at 43. As another example, the user manual for the [ ] states: "If you still have a problem, [ ]." CX-0056 ([ ]) at 1, 25. There are more such examples throughout the product literature for the accused Funai H.264 products. *See* CX-1597C (Reinman WS) at Q&A 292.

Funai also provides warranty support for the accused Funai H.264 products in the event that a device is unable to perform the accused functionality. CX-1597C (Reinman WS) at Q&A 293; *see, e.g.*, CX-0046 ([ ]) at 45; CX-0056 ([ ]) at

68. Again, there are more such examples throughout the product literature for the accused Funai H.264 products. *See* CX-1597C (Reinman WS) at Q&A 293.

Funai had actual knowledge of the '663 patent no later than March 2012, when Complainants filed the complaint in this investigation and provided infringement claim charts to Funai. The record evidence discussed above demonstrates that, following institution of this investigation, Funai continued to provide marketing and product literature to its customers. The evidence also shows that Funai continued to provide technical and warranty support to its customers after this investigation was instituted.

Therefore, if the Commission were to reverse the finding of the administrative law judge that asserted method claims 1-9 of the '663 patent are not infringed, then Funai would be liable for induced infringement of these claims.

b. Contributory Infringement

The evidence shows that the accused Funai H.264 products [

]. *See* CX-1597C (Reinman WS) at Q&A 296. In particular, [

] from the H.264 Standard in the accused Funai H.264 products is essential for viewing high-definition H.264-compliant video, and that hardware is especially made to perform processes that are alleged to infringe claims 1-9 of the '663 patent. *Id.*

Furthermore, there are no substantial non-infringing uses for [

] in the accused Funai H.264 products. *Id.* at Q&A 298. Specifically, the accused Funai H.264 products cannot fully operate ([

]) without this hardware. *Id.* Moreover, there is no evidence that the [

]. *Id.* As described earlier in connection with the discussion of induced infringement, Funai has furnished this [ ] to end users of the accused Funai H.264 products with knowledge of the '663 patent since at least March 2012, when Complainants initiated this investigation.

Therefore, it is determined that Complainants have demonstrated that Funai would be liable for contributory infringement of claims 1-9 of the '663 patent in the event it is determined that there is direct infringement of these claims.

D. Validity

1. Priority Date

The '663 patent issued from Application No. 10/770,213 (filed February 2, 2004), which is a continuation of Application No. 10/191,596 (filed July 10, 2002). JX-0007. Complainants argue that the '663 patent is entitled to the July 10, 2002 priority date of its parent application. Compls. Br. at 16-20. Respondents contend that the claims of the '663 patent are entitled only to a priority date of March 4, 2005, when the applicants allegedly added new matter during the prosecution of the '663 patent. Resps. Br. at 277-305.

Specifically, Respondents cite to a March 4, 2005 office action response from the prosecution history of the '663 patent as supporting their priority date contentions, arguing that "the '663 patent applicant added new matter in the March 4, 2005 response." *See* RX-0007C (Schonfeld WS) at Q&A 368. An analysis of the prosecution history, however, demonstrates that the evidence does not support Respondents' argument.

A review of the complete prosecution history demonstrates that no "new matter" was added to the specification of the '663 patent on March 4, 2005. The specification of the '663 patent as originally filed included two tables of index values and their corresponding UEGk

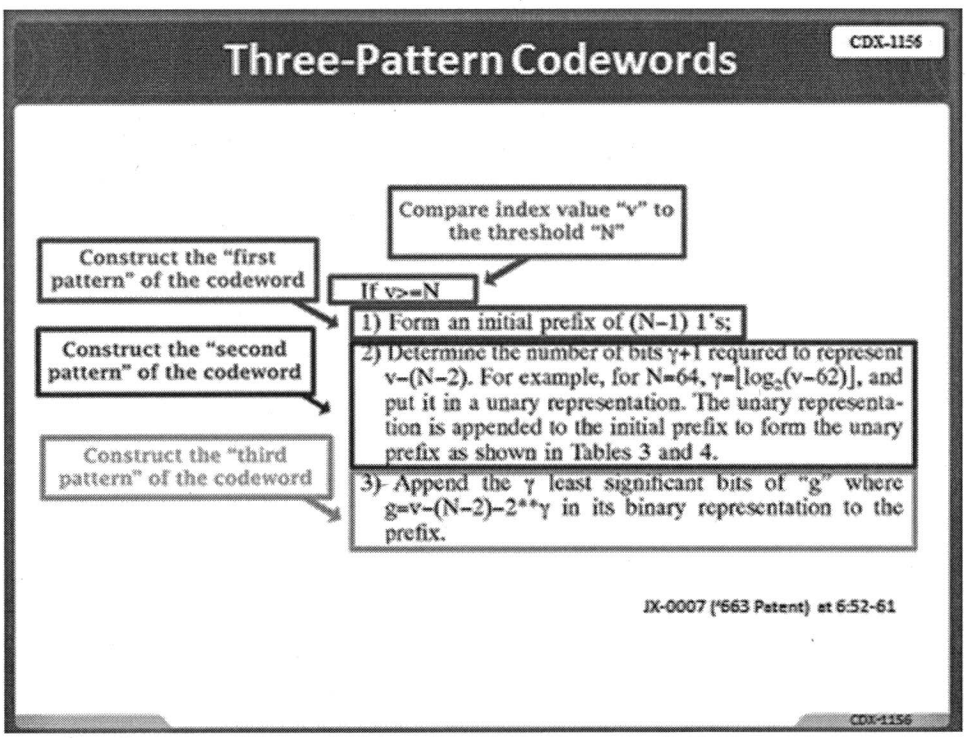
binarized codewords, *i.e.*, Table 3 and Table 4. See JX-0008 ('663 file history) at 16-17. On December 2, 2004, the PTO issued an action requiring amendment to the drawings, and specifically instructed that "[n]o new matter should be entered." *Id.* at 73. The applicant responded to that office action on March 4, 2005, indicating that "Tables 3 and 4, as originally filed, are moved into new FIGS. 5 and 6 each with an added line for clarity. Thus, no new matter has been added." *Id.* at 94. Other than the "added line for clarity," nothing else changed in Tables 3 and 4 other than the tables were turned into Figures 5 and 6. *Compare id.* at 16-17 *with id.* at 107-08; Reinman Tr. 749-750; Schonfeld Tr. 1624, 1625. Following this office action response, the PTO allowed all of the claims. JX-0008 ('663 file history) at 115. The PTOdid not reject any claims on the basis of the "added line for clarity" being new matter. *Id.*; Reinman Tr. 750.

Inasmuch as the PTO allowed the "added line for clarity" without objection, Respondents face an especially high burden in proving that the '663 patent is not entitled to the July 10, 2002 priority date of its parent application. "[I]n the context of a validity challenge based on new matter, the fact that the United States Patent and Trademark Office ('PTO') has allowed an amendment without objection 'is entitled to an especially weighty presumption of correctness' in a subsequent validity challenge based on the alleged introduction of new matter." *Commonwealth Sci. & Indus. Research Org. v. Buffalo Tech. (USA), Inc.*, 542 F.3d 1363, 1380 (Fed. Cir. 2008).

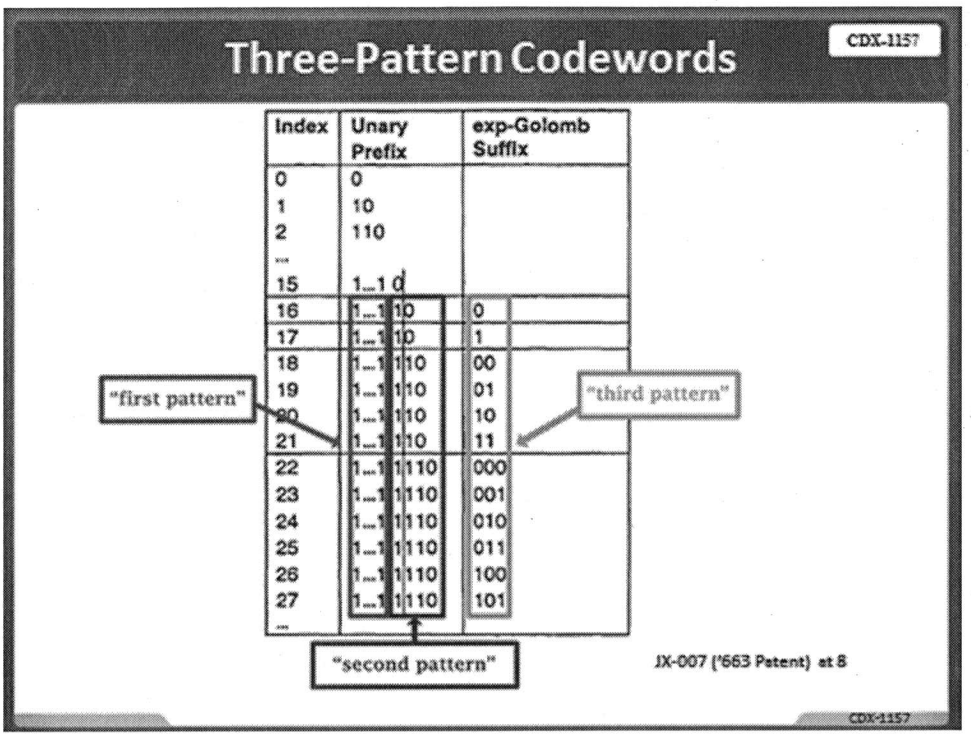
Respondents have not met their burden to adduce clear and convincing evidence that the "added line for clarity" constitutes "new matter" affecting the asserted claims of the '663 patent. Each of the asserted claims of the '663 patent involves generating an "index value" by analyzing each of three patterns used to form the corresponding "codeword" and taking certain actions as

appropriate. JX-0007 ('663 patent) at col. 7, ln. 31 – col. 8, ln. 25; CX-1644C (Richardson RWS) at Q&A 51. None of the asserted claims of the '663 patent reference or require the "added line for clarity" introduced in the March 4, 2005 office action response, as one of ordinary skill in the art can identify the three separate patterns in Figures 5 and 6 with or without the added line. *See* CX-1644C (Richardson RWS) at Q&A 51.

Specifically, the three patterns shown in Figures 5 and 6 trace back to the representative UEGk binarization process described at column 6, lines 44-63 of the '663 patent. *See id.* at Q&A 48-50. This is illustrated below in CDX-1156 (Richardson 007):

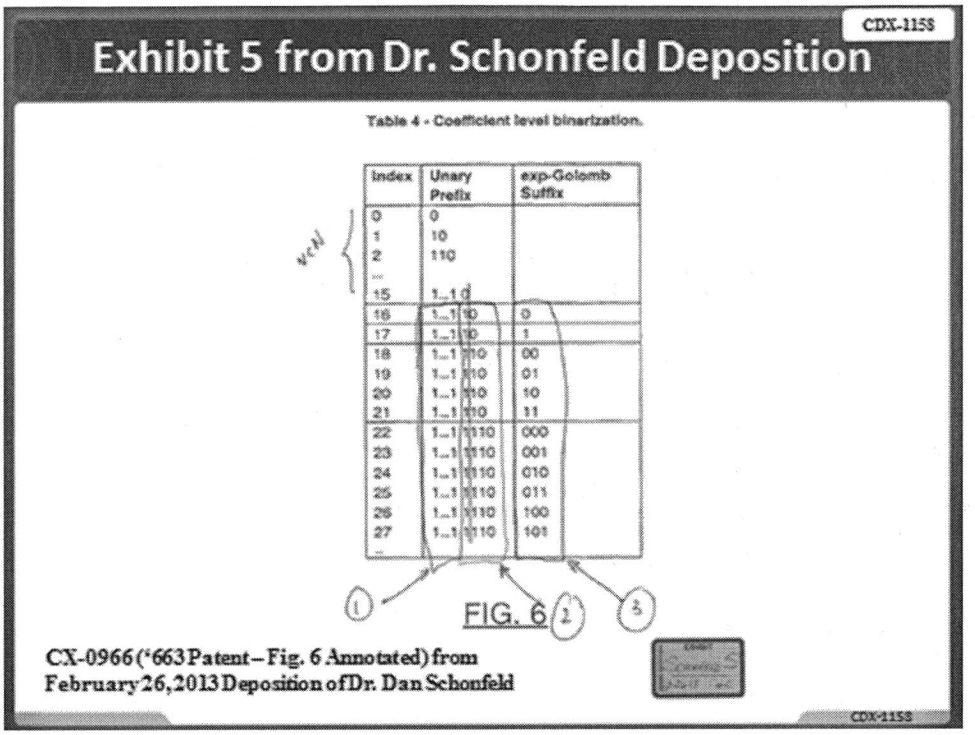


The three-pattern codewords generated from this process are found, for example, in Figure 6 (for index values above the threshold N=16). *See id.* This is seen below in CDX-1157 (Richardson 008):



Thus, the three patterns described in the asserted claims of the '663 patent would have been apparent to one of ordinary skill in the art, regardless of the presence of the vertical line. *Id.* at Q&A 51. Indeed, the "added line for clarity" does nothing more than clarify that an additional embodiment of the asserted claims can be identified in the existing tables from Figures 5 and 6. *See* Reinman Tr. 748.

Moreover, Respondents' expert Dr. Schonfeld, in reviewing column 6, lines 47-63 of the '663 patent, identified three distinct patterns in Figure 6 without any reliance on the "added line for clarity." *See id.* at Q&A 52; Schonfeld Tr. 1620-1622. This is demonstrated by Dr. Schonfeld's annotations of Figure 6 in CX-0966 ('663 Patent - Fig. 6 Annotated), shown below in CDX-1158 (Richardson 009):



See Schonfeld Tr. 1620-1622. Therefore, because none of the asserted claims of the '663 patent references or is reliant upon the "added line for clarity" from the March 4, 2005 office action, each of the asserted claims is entitled to the July 10, 2002 priority date of the '663 patent parent application. *See* CX-1644C (Richardson RWS) at Q&A 54.

2. Indefiniteness

Respondents argue that all asserted claims of the '663 patent are invalid for indefiniteness. *See* Resps. Br. at 354-55. For the reasons discussed previously with respect to the construction of the disputed claims terms, Respondents have not shown clearly and convincingly that any of the disputed claims terms are not amenable to construction or are insolubly ambiguous. Therefore, it is determined that none of the asserted claims are invalid for indefiniteness based on the disputed claim terms.

Respondents separately argue that claim 11 is indefinite because it combines function and apparatus elements in the same claim. Resps. Br. at 355-56. An apparatus claim such as claim

11 is not indefinite where it includes limitations that merely indicate the apparatus is "capable of performing the recited functions." *See Microprocessor Enhancement Corp. v. Tex. Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008). The language from claim 11 describes what the claimed "circuit" is "configured to" accomplish (*i.e.*, what it is "capable of performing"). JX-0007 ('663 patent) at col. 8, lns. 14-25. It is therefore determined that claim11 is not invalid for indefiniteness based on Respondents' argument that it combines function elements with apparatus elements.

3. Written Description

Respondents argue that "the specification of the '663 patent fails to provide a proper written description for any of the asserted claims to reasonably convey to one of ordinary skill in the art that the inventor had possession of the claimed subject." *See* Resps. Br. at 352-54. In particular, Respondents argue that the '663 specification does not provide any written description for how to perform the decoding process claimed in asserted claims 1-9 and 11. *Id.* at 353-54.

Respondents, however, have not adduced clear and convincing evidence that any asserted claim is invalid due to failure to satisfy the written description requirement.

For instance, Respondents' expert Dr. Schonfeld alleges "the '663 patent specification only describes decoding in Fig. 3 and at col. 4, lines 13-23." RX-0007C (Schonfeld WS) at Q&A 604. This testimony, however, overlooks the decoder process flow depicted in Figure 1, and the accompanying description of how such decoder "reverses the steps applied by encoder." *See* JX-0007 ('663 patent) col. 3, lns. 8-10; Fig. 1.

Moreover, Figure 4 of the '663 patent depicts "a flowchart of a process for codeword construction" using the unary/exp-Golomb ("UEGk") hybrid binarization approach disclosed in the '663 patent. *See* JX-0007 ('663 patent) at col. 6, lns. 64-65. In particular, Figure 4 discloses

a series of steps taken that are contingent on whether "the code symbol index is less than the value of the threshold." *Id.* at col. 7, lns. 1-4. As taught by the specification, the decoding of these novel UEGk codewords (*i.e.*, the process described in the asserted claims) is performed by "revers[ing] the steps" of the UEGk codeword construction shown generally in Figure 4 to arrive at the original index value. *See id.* at col. 3, lns. 8-10; CX-1644C (Richardson RWS) at Q&A 146.

Further, in column 6, lines 44-63, the '663 patent provides a "detailed description of the method for constructing such hybrid binarizations" using an encoder. CX-1644C (Richardson RWS) at Q&A 145. One embodiment of the asserted claims "reverses the steps applied by [the] encoder" during this UEGk encoding process. *See, e.g.*, Reinman Tr. 647-648; JX-0007 ('663 patent) at col. 3, lns. 8-10. Moreover, during the evidentiary hearing, testimony showed that the specification disclosed two additional embodiments of the asserted claims. Reinman Tr. 704.

Therefore, there is support in the specification of the '663 patent for the UEGk decoding process described in the asserted claims. Accordingly, it is determined that Respondents have not prevailed on their written description defense.[39]

4. Patentable Subject Matter

Respondents argue that the asserted claims of the '663 patent are invalid under 35 U.S.C. § 101 for failure to claim patentable subject matter. Resps. Br. at 317-38. As discussed below, it is determined that Respondents have not prevailed in this defense.

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[39] The GR12 Filing also indicates that this Initial Determination should address the issue of whether the asserted '663 claims are invalid for lack of enablement. GR12 Filing at 8. Respondents, however, did not address this issue in their brief. *See* Resps. Br. at 352-56; Compls. Reply at 76. Accordingly, the administrative law judge declines to make any findings on the issue of whether the asserted '663 claims are invalid for lack of enablement.

As in initial matter, all the asserted claims of the '663 patent are patent eligible under Section 101 because each satisfies the "machine" prong of the Federal Circuit's machine-or-transformation test. The Federal Circuit defines "machine" in this context as:

> [A] concrete thing, consisting of parts, or of certain devices and combination of devices. This includes every mechanical device or combination of mechanical powers and devices to perform some function and produce a certain effect or result.

SiRF Tech., Inc. v. Int'l Trade Comm'n, 601 F.3d 1319, 1332 (Fed. Cir. 2010).

A "machine," *i.e.*, a "decoder" used in the decompression of digital video, is integral to each of the asserted claims of the '663 patent. Claims 1-9 of the '663 patent are directed to "generating an index value from a codeword for digital video decoding," which is a process performed by digital video decoder. *See* JX-0007 ('663 patent) at col. 7, lns. 32-33. Similarly, in claim 11, a "decoder" is an express element of the system claim. *Id.* at col. 8, ln. 15. Moreover, each of the asserted claims involves "codewords" and "index values." As described in the '663 patent, these claimed "codewords" and "index values" represent specific data structures used exclusively in video encoders/decoders "such as transformed-quantized picture differences and motion vector residuals." *Id.* at col 4, lns. 44-45. As such, none of the asserted claims has meaning or application outside of a decoder used for decoding video.

Although satisfaction of only one prong of the Federal Circuit's machine-or-transformation test proves a claim is patent eligible under Section 101, the asserted claims of the '663 patent satisfy the second "transformation" prong as well as the first "machine" prong. The Federal Circuit has held that "the transformation of [] raw data into a particular visual depiction of a physical object on a display was sufficient" to render a particular process claim "patent-eligible" under Section 101. *In re Bilski*, 545 F.3d at 963. Moreover, the Federal Circuit

emphasized "for clarity" that "the electronic transformation of the data itself into a visual depiction . . . was sufficient; the claim was not required to involve any transformation of the underlying physical object that the data represented." *Id.*

Each of the asserted '663 claims is directed to "the transformation of [] raw data into a particular visual depiction of a visual object." *See id.* Specifically, the processes of claims 1-9 of the '663 patent are used "for generating an index value from a codeword for digital video decoding." JX-0007 ('663 patent) at col. 7, lns. 32-42. Claim 11 similarly describes a system that takes a "codeword" created by a "decoder" module and, using a "circuit," generates an "index value" from that "codeword." *Id.* at col. 4, lns. 24-25. In other words, the inventions claimed in the asserted claims take raw binarized "codeword" data received in a compressed digital video bit stream and transform the data into "index values" representing symbols "such as transformed-quantized picture differences and motion vector residuals" that instruct the decoder how to recreate the video image "that is delivered to the user." *Id.* at col. 4, lns. 44-45; col. 3, lns. 8-10. This "electronic transformation of the data itself into a visual depiction" is "sufficient" to satisfy the transformation prong of the machine-or-transformation test. *See In re Bilski*, 545 F.3d at 963.

In addition to satisfying both prongs of the Federal Circuit's machine-and-transformation test, the asserted claims of '663 patent also are patent-eligible under Section 101 because they represent narrow functional applications in the field of computer technology. "[I]nventions with specific applications or improvements to technologies in the marketplace are not likely to be so abstract that they override the statutory language [of § 101]." *Research Corp.*, 627 F.3d at 869. The asserted claims of the '663 patent each disclose a "binarization method" that "will reduce the complexity and the bitrate/size for compressing and decompressing video, images, and

signals that are compressed using binary arithmetic encoding for entropy encoding." JX-0007 ('663 patent) at col. 2, lns. 6-11. Therefore, like the patented inventions in *Research Corporation*, the inventions claimed in the '663 patent present "functional and palpable applications in the field of computer technology" and "are directed to patent-eligible subject matter." *See Research Corp.*, 627 F.3d at 868-69. As a result, "the process claims at issue, which claim aspects and applications of the same subject matter, are also patent-eligible." *See id.* at 869.

Inasmuch as the asserted claims of the '663 patent satisfy both prongs of the Federal Circuit's machine-or-transformation test for patent-eligibility, and inasmuch as the asserted claims represent narrow functional applications in the field of computer technology, it is therefore determined that Respondents have not prevailed in their Section 101 defense.

5. The JVT-C162-L Reference

Respondents argue that the JVT-C162-L proposal (RX-0740) renders obvious the asserted claims of the '663 patent. Resps. Br. at 306-09. JVT-C162-L is a proposal written the Lowell Winger, the named inventor of the '663 patent, for the Joint Video Team ("JVT") of ISO/IEC MPEG and ITU-T Video Coding Expert Group ("VCEG") entitled "Putting a Reasonable Upper Limit on Binary Expansion." RX-0740. JVT-C162-L was downloaded to a publicly available FTP site on or about May 2, 2002 in advance of the JVT 3rd Meeting in Fairfax, Virginia on May 6-10, 2002, and was therefore publicly available no later than the time of that conference. *See* JX-036C (Lindbergh Dep.) 71-73; RX-0003C (Lindbergh WS) at Q&A 26-34.

Respondents cannot prevail in their obviousness argument, however, because JVT-C162-L does not constitute prior art to the '663 patent.

As discussed previously, the asserted claims of the '663 patent are entitled to the July 10, 2002 filing date of the '663 patent parent application. Thus, in order to constitute prior art, the published reference must have been authored by someone other than the inventor of the patent. Inasmuch as Lowell Winger, the sole inventor named on the '663 patent, is also the sole author of JVT-C162-L, JVT-C162-L does not constitute prior art to the asserted claims of the '663 patent. CX-1644C (Richardson RWS) at Q&A 176.

6. The VCEG-P07 Reference

Respondents also allege that the VCEG-P07 reference renders obvious the asserted claims of the '663 patent. Resps. Br. at 309-13. VCEG-P07 is a draft of the H.264 video compression standard of the Joint Video Team ("JVT") of ISO/IEC MPEG and ITU-T Video Coding Expert Group ("VCEG"). VCEG-P07 was publicly available within a few weeks of the JVT 3rd Meeting in Fairfax, Virginia on May 6-10, 2002, as well as the VCEG16th Meeting in Fairfax, Virginia also on May 6-10, 2002. RX-0003C (Lindbergh WS) at Q&A 35-40.

Respondents cannot prevail in their obviousness argument, however, because VCEG-P07 does not constitute prior art to the '663 patent.

Given the July 10, 2002 priority date of the '663 patent, the relevant content of the VCEG-P07 must be written by someone other than the inventor of the '663 patent in order to constitute prior art. *See* 35 U.S.C. § 102(a). Respondents have not presented any evidence showing or suggesting that the relevant sections of VCEG-P07 are attributable to anyone other than Lowell Winger, the sole inventor named on the '663 patent. Therefore, VCEG-P07 is not prior art to the '663 patent, and Respondents have not prevailed in their obviousness defense.[40]

[40] Moreover, by contending that all of the asserted claims of the '663 patent are invalid over the JVT-C162-L proposal which was published "on or around May 2, 2002," Respondents have, in

VII. The '958 Patent

A. The Asserted Claims and Accused Products

Asserted U.S. Patent No. 6,452,958 ("the '958 patent") is titled, "Digital Modulation System Using Extended Code Set." JX-0003 ('958 patent). The '958 patent issued on September 17, 2002, and the named inventor is Richard D. J. van Nee. *Id.* The '958 patent relates generally to "[a] digital (de)modulation system." *Id.* at Abstract.

LSI asserts independent claims 22, 29, 32, and 35, and dependent claims 23-26 against Funai and Realtek. The relevant claims are as follows:

> **22.** A digital modulation system for modulating data bits, comprising:
>
> a serial-to-parallel converter that groups the data bits, and
>
> a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.
>
> **23.** The digital modulation system according to claim 22, further comprising a mixer that modulates a carrier signal in accordance with the chosen code.
>
> **24.** The digital modulation system according to claim 23, wherein the mixer modulates the phase of at least one carrier signal in accordance with the selected code.
>
> **25.** The digital modulation system according to claim 24, wherein the phase of the at least one carrier signal is QPSK modulated in accordance with the selected code.

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effect, admitted that Lowell Winger invented and implemented the asserted '663 patent claims no later than May 2, 2002. Inasmuch as May 2, 2002 predates the purported public availability of VCEG-P07, Respondents effectively concede that VCEG-P07 is not prior art under 35 U.S.C. § 102(a). *See* CX-1644C (Richardson RWS) at Q&A 183.

26. The digital modulation system according to claim 22, further comprising a scrambler for scrambling the group of data bits.

29. A digital modulation system for modulating data bits, comprising:

a serial-to-parallel converter that groups the data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is defined by the sequence ABAB′, such that A is a sequence of elements and B is a sequence of elements and wherein B′ is derived by inverting all elements in the sequence B.

32. A digital modulation system for modulating a group of data bits, comprising:

a scrambler for scrambling the group of data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M >N, and wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.

35. A digital modulation system for modulating a group of data bits, comprising:

a scrambler for scrambling the group of data bits, and

a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and wherein the code set is derived from a complementary code,

wherein the complementary code is defined by the sequence ABAB′, such that A is a sequence of elements and B is a sequence of elements and wherein B′ is derived by inverting all elements in the sequence B.

JX-0003 at col. 12, lns. 50-67; col. 13, lns. 1-3; col. 13, lns. 10-21; col. 13, lns. 38-46; col. 13, lns. 53-64.

Complainants accuse the following products of infringing the '958 Patent: (1) Realtek's products that are compliant or compatible with the applicable 802.11 standards described for CCK modulation; and (2) Funai's products that (a) are compatible with the applicable 802.11 standards described for CCK modulation; (b) contain at least one of Realtek's products; or (c) contain at least one of Ralink's products that are compatible with the applicable 802.11 standards described for CCK modulation. Compls. Br. at 45.[41]

Complainants provide the following table purporting to summarize Funai's products accused of infringing the '958 Patent and the '867 Patent, along with the WiFi chip supplier for each product and documentation showing 802.11 compatibility:

			]

[41] Complainants also accuse of infringement certain Funai products that contain chips from ["]). These products will be addressed separately in the section addressing Complainants' infringement arguments.

[			
			]

Compls. Br. at 46-47.

Complainants provide the following table purporting to summarize Realtek's products accused of infringing the '958 Patent and the '867 Patent, along with the documentation showing 802.11 compatibility:

[		
		]

[		

[		
		]
	]	

Compls. Br. at 47-49.

Complainants provide the following table purporting to list the Ralink products at issue with respect to the '958 Patent and the '867 Patent, along with the documentation showing 802.11 compatibility:

[		

[		
		]

Compls. Br. at 50.

B. Claim Construction

1. Level of Ordinary Skill

A person of ordinary skill in the art relevant to the '958 patent at the time of the invention had at least a master's degree in electrical engineering or a related field, and at least three years of experience and knowledge in digital communications or a related field. The Master's degree can be substituted by at least one year of training or additional work experience in the area of digital communications or a related field. *See* RX-0006C (Heegard WS) at Q&A 90-94.[42]

2. "chip"

Claim Term/Phrase	Complainants' Construction	Respondents' Construction
"chip"	No construction necessary. Alternatively, "a code bit (as distinguished from a data bit)"	"a code bit (as distinguished from a data bit"

[42] Complainants argue that a person of ordinary skill in the relevant art at the time of the invention of the '958 patent would be someone with a BSEE or equivalent and at least two years of experience in developing or implementing wireless baseband algorithms or circuits at the PHY layer. Compls. Br. at 34 (citing CX-1596C (Negus WS) at Q&A 132). The parties have not identified any way in which differences in their proposed definitions of the level of ordinary skill in the art affect issues in this investigation. *See id.*

The parties agree that the claim term "chip," as used in asserted claims 22, 29, 32, and 35 of the '958 patent, should be construed to mean "a code bit (as distinguished from a data bit)." *See* Compls. Br. at 368; Resps. Br. at 55. Therefore, the claim term "chip" is construed to mean "a code bit (as distinguished from a data bit)."

3. "code"

Claim Term/Phrase	Complainants' Construction	Respondents' Construction
"code"	No construction necessary. Alternatively, "a sequence of chips"	"a sequence of chips representing a real value"

The claim term "code" appears in asserted claims 22, 23-25, 29, 32, and 35 of the '958 patent. Complainants argue that no construction is necessary, but that if it is determined that "code" needs construction, it should be construed to mean "a sequence of chips." Compls. Br. at 368-70. Respondents argue that "code" should be construed to mean "a sequence of chips representing a real value." Resps. Br. at 55-62.

As proposed by Respondents, the claim term "code" is construed to mean "a sequence of chips representing a real value." This construction is consistent with the intrinsic evidence, and reflects the understanding of a person of ordinary skill in the art at the time of the '958 invention.

The intrinsic evidence requires restricting the claims to real codes because that is all the '958 specification discloses and allows. The stated purpose of the '958 patent, which is to overcome the limitation of "conventional M-ary keying systems" where "the number of possible codes M is not more than the code length N in chips," makes clear that the claim limitation "code" encompasses only real codes. *See* JX-0003 ('958 patent) at col. 4, lns. 61-64; Katti Tr. 1795-1797; RX-2813C (Heegard RWS) at Q&A 93 ("[I]f the 'code length N in chips' were

construed to include 'complex chips,' a greater number than N orthogonal sequences of 'complex' length N would exist; accordingly, the patent's description of both its purported problem and its purported solution would be inaccurate."); Negus Tr. 457-458. As Respondents' expert Dr. Heegard testified, "[o]ne of ordinary skill would understand that within the context of the patent, the inventor was describing real valued codes, or even integer valued codes, since there is never an inkling of a non-zero imaginary part to these codes." RX-2813C (Heegard RWS) at Q&A 90.

The only codes described in the '958 patent are set forth in Tables 1, 2, and 3 of the specification. JX-0003 ('958 patent) at col. 5, ln. 25 – col. 6, ln. 40; RX-2811C (Vojcic WS) at Q&A 36, Q&A 113; RX-2813C (Heegard RWS) at Q&A 31, Q&A 86-91. All of the codes are binary and, therefore, real. *See* RX-2813C (Heegard RWS) at Q&A 31, Q&A 86-91. Complainants' expert Dr. Negus [

]. *See* RX-2837C ([ ].) at 102-104.

By contrast, Complainants' proposed construction considers the real codes as "complex" codes with the imaginary part always set to zero. This proposed construction has already been rejected in previous litigation. RX-1345 (*Sony* Order) at 7-8; RX-2811C (Vojcic WS) at Q&A 109-11, Q&A 140; RX-2813C (Heegard RWS) at Q&A 98-99.

Moreover, the embodiments depicted in the '958 specification are designed for real codes, and not complex codes. Specifically, the system shown in Figure 3 of the '958 patent cannot accommodate complex codes, because it cannot place the imaginary part on one channel and the real part on the other channel. JX-0003 ('958 patent) at col. 7, lns. 11-34; RX-2811C (Vojcic WS) at Q&A 116-19; RX-2813C (Heegard RWS) at Q&A 86-91. Similarly, the "fallback mode" illustrated in Figures 4 and 7 requires the simultaneous transmission of the same

code on the I and Q channels, which can be achieved only with real codes, and not complex codes. *See* RX-1345 (*Sony* Order) at 7-8; JX-0003 ('958 patent) at col. 8, lns. 46-50; col. 9, lns. 52-64; RX-2811C (Vojcic WS) at Q&A 120-21; RX-2813C (Heegard RWS) at Q&A 86-91.

Complainants' proposed construction, which expands the definition of "code" to include complex codes, contradicts their agreed-upon construction of the term "chip" as "a code bit." A chip, or code bit, is "binary" and can take on only one of two values, whereas a complex chip has both real and imaginary dimensions. RX-2813C (Heegard RWS) at Q&A 43. Complex codes use "complex chips," which require more than one bit, are not binary, and therefore are not "chips." RX-2811C (Vojcic WS) at QA 121; RX-2813C (Heegard RWS) at Q&A 92, Q&A 80-84. As an example, Figure 2 of the '958 specification "shows a digital modulator 28 according to the principles of the present invention." JX-0003 ('958 patent) at col. 4, lns. 22-24. Each chip in the selected "code" is binary, inasmuch as the figure refers to "1" times the number of chips N, *i.e.*, one bit per chip. JX-0003 ('958 patent) at Fig. 2; RX-2813C (Heegard RWS) at Q&A 71-79.

Complainants also take the position that a complex code can be modulated "independently" on the I and Q channels because the real and imaginary parts of the code can be modulated "independently" on the I and Q channels. *See* CX-1641C (Katti WS) at Q&A 125. This position is not persuasive, however, because decoding complex codes requires knowledge of both the I and Q channels, so that the two channels cannot be "independent." RX-2811C (Vojcic WS) at Q&A 116, Q&A 122, Q&A 156-57; RX-0006C (Heegard WS) at Q&A 283; RX-2813C (Heegard RWS) at Q&A 87-93, Q&A 175-187. Named inventor Mr. van Nee [

].

RX-1787C ([ ].) at 119, 129-130, 150-151, 160; RX-1788C ([

].) at 33, 37-38, 49-50; RX-1789C ([ ].) at LSIAgere837-01077136-37.

Therefore, the claim term "code" is construed to mean "a sequence of chips representing a real value."

4. "a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N"

Claim Term/Phrase	Complainants' Construction	Respondents' Construction
"a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N"	No construction necessary. Alternatively, "the number of codes in the set from which a selected code is chosen must always exceed the number of chips in each code of the set"	"the number of codes in the set from which a selected code is chosen (M) must always exceed the number of bits in each code of the set (N)"

The claim limitation "a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N" appears in asserted claims 22, 29, 32, and 35 of the '958 patent. Complainants take the position that no construction is necessary for this term, but agrees to the alternative construction of "the number of codes in the set from which a selected code is chosen must always exceed the number of chips in each code of the set" in the event it is determined that construction is necessary. *See* Compls. Br. at 368. Respondents argue that the term should be construed to mean "the number of codes in the set from which a selected code is chosen (M) must always exceed the number of bits in each code of the set (N)." Resps. Br. at 62-63.

It is therefore determined that the claim limitation "a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein

M>N" should be construed to mean "the number of codes in the set from which a selected code is chosen (M) must always exceed the number of bits in each code of the set (N)."

5. "autocorrelation sidelobes suitable for multipath environments"

Claim Term/Phrase	Complainants' Construction	Respondents' Construction
"autocorrelation sidelobes suitable for multipath environments"	No construction necessary. Alternatively, "autocorrelation sidelobes that can be used in multipath environments"	Indefinite.

The claim term "autocorrelation sidelobes suitable for multipath environments" appears in asserted claims 22 and 32 of the '958 patent. Complainants take the position that no construction is necessary for this term. *See* Compls. Br. at 370, 397-98. Respondents argue that this claim term is indefinite. *See* Resps. Br. at 63, 101-05. As discussed below in the section of this Initial Determination that addresses the validity of the '958 patent, it is determined that the claim term "autocorrelation sidelobes suitable for multipath environments" is not indefinite.

C. Infringement

1. The Accused CCK Functionality of the 802.11 Standards

Complainants accuse Respondents' products of infringing the asserted claims of the '958 patent [

] *See, e.g.*, CX-1596C (Negus WS) at Q&A 135.

CCK modulation according to the IEEE 802.11b standard involves selecting complex, not real, codes. The standard describes each CCK code word as "8 complex chips" long:

18.4.6.5 Spreading sequences and modulation for CCK modulation at 5.5 Mb/s and 11 Mb/s

For the CCK modulation modes, the spreading code length is 8 and is based on complementary codes. The chipping rate is 11 Mchip/s. The symbol duration shall be exactly 8 complex chips long.

The following formula shall be used to derive the CCK code words that shall be used for spreading both 5.5 Mb/s and 11 Mb/s

$$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\} \quad (18\text{-}1)$$

where C is the code word

C = {c0 to c7}

The terms φ1, φ2, φ3, and φ4 are defined in 18.4.6.5.2 for 5.5 Mb/s and 18.4.6.5.3 for 11 Mb/s.

This formula creates 8 complex chips (c0 to c7), where c0 is transmitted first in time.

This is a form of the generalized Hadamard transform encoding, where φ1 is added to all code chips, φ2 is added to all odd code chips, φ3 is added to all odd pairs of code chips, and φ4 is added to all odd quads of code chips.

The term φ1 modifies the phase of all code chips of the sequence and shall be DQPSK encoded for 5.5 Mb/s and 11 Mb/s. This shall take the form of rotating the whole symbol by the appropriate amount relative to the phase of the preceding symbol. Note that the chip c7 of the symbol defined above is the chip that indicates the symbol's phase and is transmitted last.

CX-0116C (802.11b Standard) at CX-0166C.0723-24. Each "complex chip" is a pair of bits, one pair representing the real component of a complex value, and the other pair representing the imaginary component. RX-2813C (Heegard RWS) at Q&A 142-44; RX-2813C-1 (Heegard RWS Errata) at Q&A 2. Inasmuch as the two bits of a "complex chip" represent the real and imaginary components of a complex value, each CCK codeword represents a complex value. RX-2813C (Heegard RWS) at Q&A 142-44, Q&A 167, Q&A 169-74. Complainants' expert Dr. Negus confirmed that this is considered "complex-valued notation," in which "a 'complex value' is expressed as a real part plus an imaginary part." RX-1596C (Negus WS) at Q&A 78-80.

Inasmuch as the accused CCK functionality uses complex codes, and inasmuch as the '958 claim term "code" is construed to mean "a sequence of chips representing a real value," the

accused products do not infringe any asserted claim of the '958 patent. Complainants and their expert Dr. Negus nevertheless take the position that the accused products infringe even under the adopted construction of "code."

In support of Complainants' infringement argument, Dr. Negus testified that he has not formed an opinion on what the 802.11b standard means by a "complex chip." Negus Tr. 309-310. He also testified that he did not know the industry has a belief that CCK modulation generates a sequence of complex chips. Negus Tr. 310. When describing CCK modulation, Dr. Negus did not use the phrase "complex codes," but instead stated that CCK modulation involved a code set of 64 codes of "8 phase-modulation chips" in length. *See* CX-1596C (Negus WS) at Q&A 84-87. His own paper on CCK, however, described CCK modulation as "pick[ing] one of 64 complex codes." RX-2836 (Negus WLAN History paper) at 8; Negus Tr. 326-328. He also testified that the CCK waveform is a "complex" waveform "defined to determine the complex chip code." Negus Tr. 333-334. He further testified to several examples of references referring to CCK modulation as having "complex codes," but did not identify any reference that refers to CCK as having real codes. Negus Tr. 314-315, 334-335.

2. Complainants' Reliance on HDL Code to Show Infringement

The Hardware Description Language (HDL) code for the Accused Products provides specific functionality for the applicable 802.11 standards. CX-1596C (Negus WS) at 41, Q&A 135. HDL code is a type of source code that describes the structure and function of electronic circuits. *Id.* The CCK and synchronization functionality at issue in this investigation are implemented in the form of electronic circuits, and thus HDL code describes the relevant functionality. *Id.* Complainants' expert Dr. Negus analyzed all the HDL code that was made available to him for products that Complainants allege infringe the '958 and '867 patents. *Id.* at

Q&A 138. In some instances, counsel for Respondents stipulated that [

] *Id.* In addition to HDL code, Complainants' expert Dr. Negus also relies on product datasheets, manuals, and portions of the 802.11 Standard for his infringement analysis of the '958 accused products. *See id.* at Q&A 136.

Ralink produced a subset of the overall HDL code for its products, and Dr. Negus analyzed everything that was provided to him. *Id.* at Q&A 139. Dr. Negus found [

] to his infringement analysis of the '958 and '867 patents among the various HDL code excerpts available to him from different Ralink products. *See id.*

Realtek provided access to all of the HDL code for the entirety of all the products alleged to be part of this case. After analyzing this code, Dr. Negus identified the appropriate HDL code sections relevant to his infringement analysis. *Id.* at Q&A 140. For the '958 patent, Dr. Negus found that [

] *Id.* [

] *See, e.g.*, [ ] Tr. 1195; Vojcic Tr. 1212.

3. Claim 22

The record evidence does not show that the accused products satisfy all limitations of claim 22.

a. A digital modulation system for modulating data bits, comprising:

i. 802.11

Respondents' products are [

] CX-1596C (Negus WS) at Q&A 176; CX-0116C (802.11 Standard, Jun. 2007) at §§ 18.1.1, 18.4, 18.4.5.3, 18.4.6.3, 18.4.6.5, 18.4.6.5.3.

ii. [ ]

[

].

iii. Realtek

Datasheets for Realtek's chips state that [ ] is supported for [ ] *See, e.g.*, CX-0571C [ ]) at 5; CX-0572C [ ]) at 7; CX-0573C [ ]) at 5; CX-0576C [ ]) at 5; CX-0577C [ ]) at 5; CX-0578C [ ]) at 5; CX-0579C [ ]) at 11; CX-0580C [ ]) at 7; CX-0581C [ ]) at 7; CX-0582C [ ]) at 6; CX-0583C [ ]) at 6; CX-0584C [ ]) at 5; CX-0585C [ ]) at 5; CX-0586C [ ]) at 3; CX-0127 [ ]) at 1; CX-1596C (Negus WS) at Q&A 179.

iv. Funai

For those Funai products that interoperate with 802.11 standards devices and incorporate at least one of Ralink's chips or Realtek's chips, the same evidence described above shows that this claim element is met by structure within Funai products. *See* CX-1596C (Negus WS) at Q&A 180; CX-0587C (Funai Source Code) at FUNAI-ITC837-SC-00000073.

b. a serial-to-parallel converter that groups the data bits, and

i. 802.11

[ ] Respondents' products are [

] *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at § 18.4.6.5.3; CX-1596C (Negus WS) at Q&A 182. [

] *Id.* at Q&A 183. [

] *Id.* at Q&A 184; CX-0116C (802.11 Standard, Jun. 2007) at § 18.4.6.5.3. [

] *Id.* at Q&A 183.

ii. Ralink

[

] *See, e.g.*, CX-0561C (Ralink Source Code) at 837RALINK_SC0000001-4; CX-1596C (Negus WS) at Q&A 185.

iii. Realtek

Realtek's chips include a structure [

] The presence of a structure [

] is evident from [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002844,8,9; CX-1596C (Negus WS) Q&A 186. [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002848-49, 54; CX-1596C (Negus WS) at Q&A 186.

iv. Funai

For those Funai products that interoperate with 802.11 standards devices and incorporate at least one of Ralink's chips or Realtek's chips, the same evidence described above shows that this claim limitation is met by structure within Funai products. CX-1596C (Negus WS) at Q&A 187.

c. a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N, and

Each of the asserted claims 22-26, 29, 32 and 35 of the '958 patent recites "a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes." The term "code" is construed to mean "a sequence of chips representing a real value." As discussed above, the accused [

] Therefore, it is

determined that the accused products do not satisfy this claim limitation.

If, however, Complainants' proposed construction of "code" were adopted such that "code" meant "a sequence of chips," then the evidence shows that the accused products would satisfy this claim limitation. The following analysis sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. 802.11 – Analysis Under Alternate Construction

[ ] Respondents' products comprise structure [ ] as described above. The 802.11 Standard requires that each code is eight chips in length and there are 64 possible codes. Thus, M=64 and N=8 and M>N as required by the claim. *See* CX-1596C (Negus WS) at Q&A 188-97.

The code is chosen based on the grouped data bits. The data bits, which are grouped into di-bits, are used to select these chip sequences, or codes, to modulate signals. In particular, the grouped di-bits are mapped to "phases" denoted as "φ2, φ3, and φ4." CX-1596C (Negus WS) at Q&A 189. These phases are additively mapped to individual chips according to the rule: "φ2 is added to all odd code chips, φ3 is added to all odd pairs of code chips, and φ4 is added to all odd quads of code chips." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at § 18.4.6.5. Thus, the code selected to modulate the carrier signal is based on the grouped data bits. CX-1596C (Negus WS) at Q&A 189.

These codes are derived from a complementary code. There is a direct connection between the '958 patent and the 802.11 Standard in this regard. Equation 18-1 from the 802.11 Standard at §18.4.6.5 (CX-0116C (802.11 Standard, Jun. 2007)), which illustrates one possible

notation for representing "CCK code words," is identical to Equation 1 of the '182 patent, which is a parent patent to the '958 patent. *See* CX-0878 ('182 patent) at col. 2, lns. 21-22. Thus, the formula used to generate codes in CCK is part of the '958 patent.

Phase modulation involves mapping one or more data bits (or code bits known as "chips") to a particular phase angle of a transmitted carrier waveform. CX-1596C (Negus WS) at Q&A 193. The 11 Mb/s CCK mode of 802.11b is based on a particular form of phase modulation called "QPSK." In QPSK, one of 4 possible phase angles, each 90 degrees or $\pi/2$ radians apart, is selected as the mapping for a particular chip in the spreading sequence. *Id.* There are four possible phase angles (0, $\pi/2$, π, $3\pi/2$) mapped to four different di-bits (00, 01, 10, and 11, respectively). *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at § 18.4.6.5.3.

Complainants' expert Dr. Negus described at least two typical structural styles for implementing [ ] One exemplary structure is a "phase modulator" that outputs a phase angle for each chip in a code. CX-1596C (Negus WS) at Q&A 196. In applying this phase modulator structure to in 11 Mb/s CCK modulation, the phases "$\varphi 2$, $\varphi 3$, and $\varphi 4$" described above are "binary coded" per the grouped di-bits to phase angles $\{0,\pi/2,\pi,3\pi/2\}$ (also expressed as multiples of $\pi/2$ and written as $\{0,1,2,3\}$). *Id.*; CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5.3.

These phase angles are used to modulate carrier waves. The 802.11 standard sets forth a specific set of rules to determine how these phase angles are used to modulate carrier waves. As described above, "$\varphi 2$ is added to all odd code chips, $\varphi 3$ is added to all odd pairs of code chips, and $\varphi 4$ is added to all odd quads of code chips." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5. In addition, the 802.11 Standard requires applying an additional rotation of π (or "+2" in $\pi/2$ incremental notation) to the 4th and 7th chips. *See e.g.*, CX-0116C (802.11

Standard, Jun. 2007) at §18.4.6.5.1; CX-1596C (Negus WS) at Q&A 198. When applying these rules, a code set of 64 unique sequences of chips is realized. *Id.*

Each sequence is of length 8 chips, and each chip is a phase angle comprising two code bits. *Id.* Each of the sequence values is chosen from the set of {0,1,2,3}. *Id.* Thus, M=64 codes and N=8 chips, or thus M>N and the number of codes in the set from which a selected code is chosen always exceeds the number of chips (or code bits) in each code of the set in the "CCK 11 Mb/s modulation" mode. *Id.*

Dr. Negus also described a second exemplary structure for implementing "CCK 11 Mb/s modulation" pursuant to the 802.11 Standard. In particular, Dr. Negus described a "dual-IQ channel binary modulator" that realizes the selection of binary-coded sequences of chips in separate "I" (or "in-phase") and "Q" (or "quadrature-phase") channels. *Id.* at Q&A 203.

In an exemplary dual-IQ channel binary modulator, two separate code set selection structures are used – one for the I-channel and another for the Q-channel. *Id.* Simply put, the four phase notation chips are mapped onto I and Q values using binary arithmetic. *Id.* Binary sequences (1s and 0s) are then then transmitted on separate I and Q channels. *Id.*

Although the dual-IQ channel binary modulator comprises effectively two modulators, either the I-channel or the Q-channel structure alone meets the limitation of this claim element. *Id.* Specifically, the set of "I-channel binary codes" for 11 Mb/s CCK modulation comprises 40 unique sequences of chips wherein each sequence is of length 8 chips and each chip comprises one code bit. *Id.* at Q&A 206. Thus, for the I-channel structure, this results in M=40 codes and N=8 chips, and thus M>N. *Id.*

In another variant of the dual-IQ channel binary modulator, the four phases of QPSK are then mapped to signed values of I and Q by the simple relationships "I=sin(phase)" and

"Q=cos(phase)." *Id.* This "dual-IQ channel signed binary modulator" also results in M=40 codes and N=8 chips for the I channel and M=64 and N=8 chips for the Q channel, with the result that M>N. *Id.*

ii. Ralink – Analysis Under Alternate Construction

[

] *Id.* Thus, Ralink's chips comprise a structure that is "a modulator that chooses a code having N chips in response to the group of data bits, the code being a member of a code set that includes M codes, wherein M>N."

For example, [

] *Id.* at 61. [

] *Id.* [

] *Id.*; CX-0561C ([

]

[

] *See, e.g.*, JX-0032C ([.]

[

] *See* CX-1596C ([

] *Id.* [

] *Id.*

[

] *Id.*

[

] *Id.*; CX-0561C ([

CX-1596C (Negus WS) at Q&A 213.

Id.

[

] *Id.* at Q&A 215.]

iii. Realtek – Analysis Under Alternate Construction

Realtek's HDL code shows that [

] is present in Realtek's chips. *Id.* at Q&A 216. Thus, Realtek's chips also

comprise a structure [

]

Structure described by [

] *Id.*; CX-0298C (Realtek Source Code) at REA837ITC-SC-00000285; REA837ITC-SC-00002853,4,7-9. [

] CX-1596C (Negus WS) at 64-65, Q&A 218.

[

] CX-1596C (Negus WS) at Q&A 218.

[

] *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5; CX-0298C (Realtek Source Code) at REA837ITC-SC-000002854,57-59; CX-1596C (Negus WS) at Q&A 219.

Elements of [ ] structure within the Realtek HDL code [

]

Id. [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002857; REA837ITC-SC-00000285; REA837ITC-SC-00002853,4,7-9; CX-1596C (Negus WS) at Q&A 219.

[

]

CX-1596C (Negus WS) at Q&A 219. [

] *Id.* [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002857-59; CX-1596C (Negus WS) at Q&A 219.

iv. Funai – Analysis Under Alternate Construction

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips. CX-1596C (Negus WS) at Q&A 221.

d. wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments.

A "complementary code" can be generated, *e.g.*, by composing sequences in the form "{A,B,A,B'}" where B' is the inverse of B. If A={1,1}, B={1,-1}, and B'={-1,1}, then ABAB'={1,1,1,-1,1,1,-1,1}. This is the code from which CCK codes are derived. *See* CX-0882 ('732 patent) at col. 5, lns. 1-21; CX-1596C (Negus WS) at Q&A 73.

As set forth above, the claim term "code" was construed to mean "a sequence of chips representing a real value." If, however, Complainant's proposed construction of "code" were adopted such that the term meant "a sequence of chips," then the evidence shows that the accused products would satisfy the claim limitation "wherein the code set is derived from a complementary code that provides autocorrelation sidelobes suitable for multipath environments."

The following analysis sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. 802.11 – Analysis Under Alternate Construction

The 802.11 Standard explicitly states that CCK code words are "based on complementary codes." CX-0116C (802.11 Standard, Jun. 2007) at §§18.4.6.5. Codes are selected from a code set "derived from a complementary code" because the codes are formed by combining "generalized Hadamard transform encoding" and a "cover sequence" that is recognizable as {1,1,1,-1,1,1,-1,1}. *See* CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5; CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5.1; CX-1596C (Negus WS) at Q&A 232. This 802.11b cover sequence is a complementary code. CX-1596C (Negus WS) at Q&A 232.

The 802.11 standard states that the purpose of the "cover sequence" (or complementary code) is "to optimize the sequence correlation properties and minimize dc offsets in the codes." CX-0116C (802.11 Standard, Jun. 2007) at §18.4.6.5.1. Since the "cross-correlation properties" of the code set are generally made acceptable by the "Hadamard transform encoding" process, the purpose of using the "cover sequence" (or complementary code) to "optimize the sequence correlation properties" is to provide low autocorrelation sidelobes suitable for multipath environments. CX-1596C (Negus WS) at Q&A 233.

The evidence shows that applying the cover sequence in fact results in low autocorrelation sidelobes. When the peak autocorrelation sidelobes of codes that meet the requirements of the 802.11 Standard at §18.4.6.5.3 are compared with and without application of the "cover sequence" (or complementary code) {1,1,1,-1,1,1,-1,1}, the peak autocorrelation sidelobes with the complementary code are lower than those without. CX-1596C (Negus WS) at Q&A 236. It is well known that for the complementary code {1,1,1,-1,1,1,-1,1} applied to the

"generalized Hadamard transform encoding," the resultant autocorrelation sidelobes range from about zero to less than one half of the code length when the shifted chips are time-aligned. *Id.* Per the explicit example given in the '958 patent, this range corresponds to a "small" "multipath performance degradation." *See* JX-0003 ('958 patent) at col. 4, lns. 1-6.

The drafters of the 802.11b standard chose the complementary code {1,1,1,-1,1,1,-1,1} as the "cover sequence" precisely because this provided low autocorrelation sidelobes due to its "sequence correlation properties" so as to create a standard suitable for "multipath environments." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §§5.2.4, 14.9, 19.7.2.1, 19.7.2.1.1, 19.7.2.1.3; CX-1596C (Negus WS) at Q&A 237.

ii. Ralink – Analysis Under Alternate Construction

[

] *See, e.g.*, CX-0561C (

] *See, e.g.*, CX-0561C ([

] *Id.*

[

] *See, e.g.*, CX-0561C ([

; CX-1596C .

] *Id.*

] CX-1596C .

iii. Realtek – Analysis Under Alternate Construction

[

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002857,8; CX-1596C (Negus WS) at Q&A 240. As with Ralink's chips, [

] CX-1596C (Negus WS) at Q&A 241. This complementary code provides for "autocorrelation sidelobes suitable for multipath environments" for at least the reasons described generally for such complementary codes in the 802.11 standard. *Id.*

iv. Funai – Analysis Under Alternate Construction

For those of Funai's products that interoperate with 802.11 standards devices and contain at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips and is met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 242.

4. Claim 23

The record evidence shows that the accused products do not satisfy all limitations of claim 23.

a. The digital modulation system according to claim 22,

As shown above, the accused products do not satisfy all limitations of asserted claim 22 under the adopted claim constructions.

b. further comprising a mixer that modulates a carrier signal in accordance with the chosen code.

As set forth above, the claim term "code" was construed to mean "a sequence of chips representing a real value." If, however, Complainant's proposed construction of "code" were adopted such that the term meant "a sequence of chips," then the evidence shows that the accused products would satisfy the claim limitation "a mixer that modulates a carrier signal in accordance with the chosen code." The following analysis sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. 802.11 – Analysis Under Alternate Construction

The 802.11 standard for 11 Mb/s CCK modulation requires that the selection of codes in response to grouped data bits "(d0 to d7; d0 first in time)" is at least a phase modulation using QPSK for a 2.4 GHz carrier signal. *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §§18.1, 18.4.6.5, 18.4.6.5.3; CX-1596C (Negus WS) at Q&A 249. As discussed above, the selected codes are used to modulate carrier signals to transmit information. Thus, this limitation is met under the 802.11 Standard.

ii. Ralink – Analysis Under Alternate Construction

[

] *See, e.g.*, CX-0562C

CX-0563C

; CX-0564C ; CX-0565C

CX-0566C ; CX-0567C ; CX-0568C

; CX-0569C ; CX-0570C ;

CX-1596C (

CX-0562C

CX-0563 ; CX-0566C

; CX-0567C ; CX-0568C

; CX-0569C ; CX-0570C ;

JX-0015C ; CX-1596C .]

iii. Realtek – Analysis Under Alternate Construction

Datasheets for certain of Realtek's chips describe [

] *See, e.g.*,

CX-0571C [at 8; CX-0572C [ ]) at 11;

CX-0573C [ ]) at 8; CX-0575C [ ]) at

8; CX-0576C [ ]) at 9; CX-0577C [ ]) at

9; CX-0578C [ ]) at 10; CX-0579C [ ]) at 16;

CX-0580C [ ]) at 57; CX-0581C [ ]) at 41;

CX-0582C [ ]) at 37; CX-0583C [ ]) at 38;

CX-0584C [ ]) at 9-10; CX-1596C (Negus WS) at Q&A 252. An [

] indicates that the [ ] comprises a [ ] to perform such [

] *See, e.g.*, CX-0572C [ ]) at 180-194; CX-1596C (Negus WS) at Q&A 252.

iv. Funai – Analysis Under Alternate Construction

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips and is met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 254. Even if a Funai product comprised an older Realtek chip that may not meet the recited limitation due to a lack of RF circuitry, such RF circuitry would still necessarily be present in Funai's products even if supplied by some other non-accused Realtek chip or product(s) from another chip supplier. *Id.*

5. Claim 24

The record evidence shows that the accused products do not satisfy all limitations of claim 24.

a. The digital modulation system according to claim 23,

As shown above, the accused products do not satisfy all limitations of asserted claim 23 under the adopted claim constructions.

b. wherein the mixer modulates the phase of at least one carrier signal in accordance with the selected code.

As set forth above, the claim term "code" was construed to mean "a sequence of chips representing a real value." If, however, Complainant's proposed construction of "code" were adopted such that the term meant "a sequence of chips," then the evidence shows that the accused products would satisfy the claim limitation "the mixer modulates the phase of at least one carrier signal in accordance with the selected code." The accused products satisfy this claim limitation for the same reasons discussed above with respect to claim 23. In particular, the mixer