('757 patent, claim 1.) Plainly, a POSITA would immediately know control inputs receive control signals as is apparent from the specification. (*Id.*, citing'757 patent at 3:7–9.) Continuing, the Staff contends a POSITA would understand the set of control signals received by the control inputs can include any number of control signals, even as few as one. (*Id.*) Nor, as the Staff points out, is there any evidence the applicant disclaimed the receipt of a single control signal as excluded from the claimed set of control signals. (*Id.*) Replying to Macronix's null set argument, Staff accurately notes that since the claim explicitly recites "a first state of control signals in the set of control signals," the possibility of a null set is negated. (*Id.*)

In responding to Complainants assertion that use of the phrase "enable or inhibit a response or operation" introduces ambiguity, the Staff notes that Complainants argue their construction "requires only that the control signals control the operations of the integrated circuit, and does not leave ambiguities about whether other information such as commands or addresses may also be used in the operation." (*Id.*, citing CMIB at 47.) The Staff rejects that its construction is likely to cause confusion or ambiguity to a POSITA because such a person would already understand what a control signal is and thus understand that "commands and addresses received on the address inputs or data input/outputs" are separate and distinct from the control signals. (*Id.* citing the '757 patent at 3:7–19, 3:40–61.) Nevertheless, the Staff does assert the phrase "for controlling operations of an integrated circuit" would be understood to be nearly equivalent/identical to the phrase "that enable or inhibit a response or an operation" in the context of the '757 patent. (SMIB at 25.) Thus, even though the Staff argues its construction is clearer, it is willing to accept an alternative interpretation of the plain and ordinary meaning for "set of control signals" to be a "set of signals for controlling operations of an integrated circuit." (*Id.*)

During the Markman hearing, Respondents' counsel and I engaged in a detailed and specific discussion of Respondents' arguments. (Tr. 273-296.) To my mind, the Respondents did

not materially alter their argument as identified by the Staff, *i.e.*, that the construction for the disputed term must include a reset/power down signal and a write protect signal, wherein Respondents cited several examples of disclosed embodiments from the specification. (SMIB at 25, citing RMIB at 39–40; and *see* Tr. at 276:5-7; 279-284). Regardless, the Staff contends Respondents' argument contravenes Federal Circuit case law wherein the court cautioned against reading in particular examples or embodiments found specification as claims limitations. *Phillips*, 415 F.3d at 1323; *Kara Tech.*, 582 F.3d at 1348 ("The patentee is entitled to the full scope of his claims, and we will not limit him to his preferred embodiment or import a limitation from the specification into the claims."). (SMIB at 25.)

The Staff also observed that when Respondents argued "[t]here is no way to 'inhibit the sector erase and program operations in a particular sector in response to . . . a first set of control signals in the set of control signals,' as required by the claims . . ." without utilizing the reset/power down signal and the write protect signal, Respondents missed the point about what a POSITA would understand. (*Id.*, citing RMIB at 40.) The Staff noted that even were Respondents' argument correct, a POSITA would still readily understand the context of claims 1 and 2 means the set of control signals would [necessarily][3] include a reset/power down signal and a write protect signal. (*Id.*) Hence, a POSITA would know and appreciate the foregoing, simply from the context of the claims themselves, which refer to inhibiting (claim 1) or enabling (claim 2) the sector erase and program operations, which Respondents argue can only occur utilizing a reset/power down signal and a write protect signal. (SMIB at 25-26.)

[3] My addition. I find it is obvious.

Moreover, the Staff points out that in the context of claim 7, the additional limitation Respondents insist upon would only add unnecessary verbiage that would have no bearing on the understanding or interpretation of the claim, to wit:

> The integrated circuit of claim 1, wherein the integrated circuit receives a supply potential of about five volts or less, and the first state of the set of control signals includes a first control signal having a voltage state less than or equal to the supply potential and a second control signal having a voltage state less than or equal to the supply potential.

(SMIB at 26, citing '757 patent, claim 7.) Hence, Staff asserts I should reject Respondents' proposed construction, to the extent it seeks to include the additional limitation that the control signals "includ[e] a reset/power down signal and a write protect signal," because it is unnecessary and because it imports specific embodiments from the specification into the claims as limitations. (*Id.*) I agree with the Staff.

The Staff's closes by addressing Respondents' contention that the Staff's construction is overly broad and inconsistent with the intrinsic record.[4] (*Id.*) Respondents argue that the control signals must include a reset/power down signal and a write protect signal that enable or inhibit a sector erase or program operation, because without a recitation of these elements, the sector erase or program operations recited in the claims cannot be inhibited or enabled. (RMIB at 41.) The Staff notes, as it has already explained, that since these operations cannot be accomplished by anything other than a reset/power down signal and a write protect signal, a POSITA would recognize those signals are necessary to be included in the "set of control signals." (*Id.*)

The Staff notes, as do I, that there is nothing in the patent or science that limits the signals available to a: (1) reset/power down signal or a (2) write protect signal.[5] (*Id.*) The Staff asserts those two types of signals are singled out by Respondents because claims 1 and 2 refer to

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[4] Respondents make the same allegation about the construction advocated by Macronix. (RMIB at 41.)

[5] A Macronix concern. (Tr. at 300-301.)

inhibiting and enabling the sector erase and program operations. (*Id.*) Hence, according to the Staff, were Respondents' argument valid, there is no reason to construe the language as Respondents advocate, because under the Staff's construction, the "set of control signals" recited in claims 1 and 2 "would inherently include a reset/power down signal and a write protect signal in order to accomplish the inhibiting and enabling the sector erase and program operations recited in those claims." (SMIB at 47.)

In consideration of the foregoing, I find the Staff's proposed plain and ordinary construction is not overly broad and is consistent with the intrinsic record. (Tr. at 297.) (Complainants accept a plain and ordinary construction. (Tr. 300-301.)) Construing the term to have its plain and ordinary meaning gives meaning to the term "control signals" that is understandable to a POSITA without diminishing its scope while allowing the remainder of the claim to provide the necessary metes and bounds. Therefore, I must not and will not incorporate limitations from the remainder of the claim (or any embodiments from the specification) into the construction of a term that is well understood by a POSITA. I agree with the Staff that Respondents' proposed construction would, at the best, do nothing more than inject redundancy in claim language and potentially obscure the plain and ordinary meaning, *i.e.*, "set of signals that enable or inhibit a response or an operation." Thus I am not convinced the Staff's equivalent or alternative interpretation which is a "set of signals for controlling operations of an integrated circuit" is necessary under the circumstances as an equivalent interpretation of the plain and ordinary meaning of the disputed term. However, I do tend to agree it means the same thing.

VI. The '324 Patent

A. Overview

The '324 patent is titled "Serial Peripheral Interface and Method for Data Transmission." The USPTO issued patent '324 on December 25, 2012 from U.S. Patent Application No.

13/362,801 ("the '801 application"), which was filed on January 31, 2012. The patent is subject to a terminal disclaimer, shortening the term of the '324 patent to expire on the same date as the expiration of U.S. Patent No. 7,788,438 (*i.e.*, June 25, 2028)—a parent patent to the '324 patent. Through several intervening continuation applications, the '801 application claims priority to Provisional Patent Application No. 60/851,312, filed on October 13, 2006. The '324 patent has 15 claims, of which Claims 1 and 8 are the independent. Macronix asserts Claims 1, 2, 7, 8, and 15 in this Investigation. *See* 79 Fed. Reg. 45221. The '324 patent is directed to a serial peripheral interface having improved data transmission behavior. (Complaint, ¶ 69.)

B. Disputed Claim Term

1. "transmit[ting] the instruction, the address or the read out data"

Respondents identified "transmit[ting] the instruction, the address or the read out data" as a term that requires construction. This term appears in claims 7 and 15 of the '324 patent. The parties have each proposed the following constructions:

Complainants	Respondents	Staff
ordinary meaning –OR – "transfer the instruction, the address or the read out data"	Indefinite	no construction necessary—*i.e.*, "transmit[ting] the instruction, the address, or the read out data"

Macronix and the Staff share almost the same views on this disputed term. However, Macronix proposes a construction substituting the synonym "transfer" for "transmit," leaving the remainder of the disputed phrase intact. This is interesting, for Macronix admitted elsewhere in its brief that the Federal Circuit holds that "merely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction." (CMIB at 11, *citing C.R. Bard*, 388 F.3d at 863.) The Staff alleges, and I agree that there is no reasonable dispute as to the plain meaning of the term "transmit[ting] the instruction, the address or the read out data." (SMIB at 28.) Thus, because Macronix's construction fails to meaningfully clarify the

disputed term and could be argued to create more uncertainty by replacing the term "transmit," which is a commonly used and well-understood term in the electronics industry, there is no reason to consider it.

Respondents offer no construction and contend that the term is indefinite based on the fact that in a parent patent, the applicant amended similar claim language to overcome an indefiniteness rejection by the Examiner, because it was "unclear as to whether the plurality of pins are being used to transmit or receive the instruction to/from the integrated circuit." (RMIB at 44-45; RSMB at 2-4.) The key to Respondents' argument is that during the prosecution of the parent U.S. Patent No. 8,135,896, the Examiner found that one element of the claim recited "integrated circuit receives the instruction," while another element of the same claim stated that the pins are for "transmitting an instruction," thus making it "unclear as to whether the plurality of pins are being used to transmit or receive the instruction to/from the integrated circuit." (Exhibit 4 at SP922_00283055.)

Macronix contends that the claims at issue in the application for the parent '896 patent are different from those at issue in the asserted '324 patent. (CMIB at 55–56; CMSB at1, and 3-5.) Complainants contend that the '896 patent issue could not be resolved by the Examiner because claim 1 was originally filed to recite "a plurality of pins coupled to the integrated circuit for transmitting an instruction, an address or a read out data," while claim 2, which depended from claim 1, recited "wherein the integrated circuit receives the instruction" through the plurality of pins. (CMIB at 55.) In responding to my request for further briefing Macronix argued:

> Spansion's Markman presentation included a table comparing the originally pending claims in the 826 prosecution to claim 7 of the '324 patent. [Ex. B, Respondents' Slide 8]. But even this chart shows substantial differences between the claims rejected for indefiniteness in the '896 patent and the claims issued in the '324 patent.
>
> First, and foremost, in the '896 application, the challenged word "transmit" was not used solely in connection with an element that recited timing (rising edge,

falling edge, or both) but instead appears at the outset to describe the function of the pins generally (see first element after preamble). In contrast, in the '324 patent, claim 7 is structured so as to first clearly recite what is received and what is sent and then uses "transmit" solely in the context of setting the clock timing. This difference alone can explain why Examiner Faisal had no trouble understanding the scope of claim 7 of the '324 patent with reasonable certainty, even after rejecting original claim 2 of the '896 application. Second, claim 7 of the '324 patent, unlike the '896 patent's claims, expressly recites a sequence of operations – specifically reciting that an address is received "after receiving" the instruction.[footnote omitted] This additional clarification is absent from the '896 patent's claims that were rejected by Examiner Faisal.

Third, Spansion's chart wrongfully implies that Macronix responded to the rejection in the '896 prosecution by just changing the word "transmit" to "transceive," when in fact, the prosecution was much more complex. By the time Macronix made the change to "transceive," the then-pending claims had morphed into something with numerous differences from claim 7 of the '324 patent, including completely rewriting the independent claim elements at issue, and making further amendments so that the final allowed version of the claim with the word "transceive" bears little resemblance to claim 7 of the '324 patent.[footnote omitted] The multiple changes Macronix made to the '896 patent's pending claims hardly amount to a "clear disavowal" that forever precludes Macronix from ever using the word "transmit" in any context, especially here where claim 7 itself recites what is received and what is sent.

The differences between claim 7 of the '324 patent and the rejected claims of the '896 patent application, and the complexity of the claim amendments made by Macronix during the '896 prosecution fall far short of a clear "disavowal" of anything by Macronix. More fundamentally, the fact that Examiner Faisal handled both prosecutions and clearly understood the challenged claims of the '324 patent with "reasonable certainty" undermines Spansion's position. Indeed, the combination of the Examiner's ability to understand the claim language at issue and Spansion's failure to introduce any expert testimony to the contrary bars Spansion from climbing the high barrier imposed by *Nautilus*.

Finally, to the extent Spansion has invoked the concept of the "public notice" function of prosecution histories, it has that concept backwards. "Public notice" regarding the scope of the claims of the '324 patent are provided by the words of the claim, the specification of the '324 patent, and the prosecution history of the '324 patent itself. A person of skill in the art reading the '324 patent's prosecution history would see that Examiner Faisal plainly understood the scope of the "transmit" claim element because he mapped it to prior art when making prior art based rejections and he never once raised an indefiniteness rejection or concern about the language in claims 7 and 15.

(CMSB at 3-5.)

In the Staff's Supplemental Brief, in addition to successfully distinguishing case law cited by Respondents in support of its indefiniteness argument, the Staff wrote:

> To the extent the applicant acquiesced, moreover, the surrender was limited to the indefiniteness of original application claim that was rejected by the examiner during the prosecution of the parent '896 patent. The indefiniteness of a claim may not be considered in piecemeal format by analyzing a single claim term divorced from the claims and the specification. *See* MPEP § 2173.02(II). The examiner of the '324 patent-in-suit was also the examiner of the parent '896 patent. The application that issued as the parent '896 patent was filed on August 5, 2010 and issued on March 13, 2012. The application that issued as the '324 patent-in-suit was filed on January 31, 2012 and issued on December 25, 2012. Respondents' argument that the term "transmit" is indefinite begs the question why the examiner did not reject claims reciting "transmit" in the course of the prosecution of the '324 patent.
>
> One possible explanation for the non-rejection in the '324 patent is simply that the examiner, in viewing the totality of the application for the '324 patent, understood the scope of the claims reciting "transmit" with reasonable certainty, even though he rejected other claims containing the word "transmit" in the application for the parent '896 patent. Thus, the Staff submits that there should not be a presumption that claims 7 and 15, which recite the term "transmit[ting] the instruction, the address or the read out data," is indefinite.
>
> However, the Staff agrees with the Respondents to the extent that they argue that Macronix may have disclaimed a broad definition for "transmit" during the course of the prosecution of the parent '896 patent. Macronix, in amending the then-pending claims in the application for the '896 patent from "transmit" to "transceive," argued that "[t]he word 'transceive' means to 'transmit and receive'." *See* Exhibit A (June 22, 2011 Amendment) at SP922_00283029. In the Staff's view, by this statement, Macronix implicitly disclaimed a broad interpretation of the term "transmit" in the '896 patent and all related patents, including the '324 patent. Thus, the term "transmit" as used in the '324 patent must be given in its plain and ordinary meaning—*i.e.*, to exclude receiving. In the Staff's view, this is the extent of the disclaimer or acquiescence by Macronix committed during the prosecution of the parent '896 patent. The disclaimer or acquiescence does not extend to finding that any claim reciting the term should be found indefinite, as Respondents suggest.

(SMSB at 4-5)

Even if I were not persuaded by the Staff's argument and Macronix's recitation of the facts, I would still not determine this language in dispute is indefinite at this stage of the proceedings. As I wrote earlier in this Order rejecting a similar request for the '826 patent:

> [W]hat Respondents are actually asking me to do is make a substantive ruling with a dispositive effect. In other words, Respondents should have moved for summary determination supported by statements from persons of ordinary skill in the art. Since the Commission has held that Markman Orders are not subject to review, I cannot accomplish what Respondent wants.

(*Supra* at 15.) Thus, any expectation by Respondents that I can rule in their favor on this issue is erroneous.

For purposes of the claim construction hearing, the issue is whether the phrase identified by the parties can be construed and, if so, what the proper construction is. I have no indication that any of the parties dispute the plain and ordinary meaning of "transmit[ting] the instruction, the address or the read out data." As argued by the Staff, I find the term does not need construction for it is clear on its face. (*See* SMIB at 29.) In passing, I do note that I agree with the Staff that the word "transmit" does not mean "receive" and that the scope of the word "transmit" is less than the scope of the word "transceive." (*See* SMSB at 5.)

With respect to the invalidity issue, it is plain to me that without the benefit of expert testimony, I cannot possibly determine if the "patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus*, 134 S.Ct. at 2129. Also, I note I am not persuaded by Respondents' acquiescence arguments and agree with the analysis of the Staff concerning the applicability of the case law relied upon by Respondents. Similarly, I find Macronix's exposition of the facts to be more persuasive.

VII. The '330 Patent

A. Overview

The '330 patent is titled "Method and System for Enhanced Read Performance in Serial Peripheral Interface." The USPTO issued the '330 patent on December 25, 2012 from U.S. Patent Application No. 11/970,468 ("the '448 application"), which was filed on January 7, 2008. The term of this patent is extended under 35 U.S.C. § 154(b) by 397 days. The '448 application does not claim an earlier priority date. The '330 patent contains 12 claims. Claims 1 and 9 are the

independent claims. Macronix asserted claims 1–3 and 8–11 in this Investigation. *See* 79 Fed. Reg. 45221. The '330 patent is directed to providing enhanced data read performance in an integrated circuit. (Complaint, ¶ 78.)

B. Disputed Claim Terms

1. "performance enhancement indicator"

Respondents and the Staff identified "performance enhancement indicator" as a term that requires construction. This term appears in claims 1, 3, 8, 9, and 11 of the '330 patent. The parties have each proposed the following constructions:

Complainants	Respondents	Staff
"signal indicating that an enhanced read operation is to be performed"	"a signal that initiates an enhanced read operation"	"a signal that initiates an enhanced read operation"

The Parties' Positions

Macronix argues that properly construed the term "performance enhancement indicator" is a "signal indicating that an enhanced read operation is to be performed." (CMIB at 59-60.) Complainants assert that the dispute between the parties centers around whether a "performance enhancement indicator" must actually initiate an enhanced read operation or whether the claim should not be so limited. (*Id.* at 60.) Macronix argues the language of the claims does not suggest that a performance enhancement indicator must actually initiate an enhanced read operation. (*Id.*) Complainants argue the claims provide no requirement that the performance enhancement indicator, by itself, determines whether an enhanced read operation is to be performed or actually initiate the enhanced read operation. (*Id.* at 60-61.) Macronix also argues the specification discloses that determining whether to perform an enhanced read operation may be based on information other than the performance enhancement indicator. (*Id.* at 61.)

Respondents argue that the term "performance enhancement indicator" is "a signal that initiates an enhanced read operation." (RMIB at 47-48.) Respondents argue that its proposed construction clarifies that the performance enhancement indicator causes the enhanced read operation to occur. (*Id.* at 48.) Respondents argue its interpretation is supported by the language of the claims, specifically claims 1 and 9, the specification, and the prosecution history. (*Id.*) Respondents argue that during prosecution the applicants argued that certain prior art did not teach "determining whether to perform an enhanced [sic] operation based on the performance enhancement indicator, in the manner recited in" then-pending claim 20, which issued as claim 1. (*Id.*) Thus, Respondents argue the applicants underscored that the performance enhancement indicator causes the chip to enter an enhanced read operation. (*Id.* at 49.) Respondents argue that complainants' construction appears to treat the performance enhancement indicator as passive information that merely reflects the fact that an enhanced read operation will be performed. (*Id.* at 49-50.) Respondents assert that complainants' proposed construction is inconsistent with the specification and file history as it would allow for something other than the performance enhancement indicator to cause the chip to enter into an enhanced read mode. (*Id.* at 50.)

The Staff argues that the term is properly construed to mean "a signal that initiates an enhanced read operation." (SMIB at 30.) The Staff argues that Macronix's proposed construction should be rejected because it suggests that the signal alone is not necessarily sufficient to initiate the process of an enhanced read operation. (*Id.* at 31.) The Staff argues that the language of claims 1 and 9 make clear the performance enhancement indicator is a signal that initiates an enhanced read operation. (*Id.*)

Discussion

The term "performance enhancement indicator" appears in claim 1 in the following context:

> A method for conducting a read operation in an integrated circuit, the method comprising:
>
> ...
>
> receiving a first performance enhancement indicator ... for determining whether an enhanced read operation is to be performed; and
>
> performing the enhanced read operation, in case of determining that the enhanced read operation is to be performed.

('330 patent, claim 1.) In claim 9, the disputed term appears as follows:

> A system for enhanced data read, the system comprising one or more components configured to:
>
> ...
>
> receive a first performance enhancement indicator ...;
>
> determine whether an enhanced read operation is to be performed based upon the first performance enhancement indicator; and
>
> perform the enhanced read operation in case of determining that the enhanced read operation is to be performed.

('330 patent, claim 9.) Contrary to Respondents and Staff's argument, I do not find the language of the claims compels an interpretation that the performance enhancement indicator causes (*i.e.*, initiates) the enhanced read operation to be performed. Both Respondents and the Staff read the claim language too narrowly.

Claim 1 requires that a performance enhancement indicator is received for determining whether an enhanced read operation is to be performed. A plain reading of the language "for determining whether an enhanced read operation is to be performed" could mean, as Staff and Respondents would like me to interpret it, that the performance enhancement indicator, itself, determines whether an enhanced read operation is performed. Or, the language could be read to mean, as Macronix would like me to interpret it, that the performance enhancement indicator may

be used along with additional information to determine whether to perform an enhanced read operation. Claim 9 requires receiving a performance enhancement indicator and then determining whether to perform an enhanced read operation based on the performance enhancement indicator. Similar to claim 1, the language "based upon the ... performance enhancement indicator" could be read to support either Respondents and the Staff's argument, or Macronix's argument. However, I would say in this instance the plain language favors Macronix's argument as Respondents and the Staff are really asking me to interpret "based upon" as "based directly upon."

The correct claim construction is the one that most closely aligns with the language of the claims as read in light of the specification and prosecution history. Here, the specification strongly supports Complainants' proposed construction. In particular, the specification states:

> The method also includes performing an enhanced read operation, if it is determined that the enhanced read operation is to be performed based on *at least information associated with the performance enhancement indicator.*

(*Id.* at 1:66-2:3 (emphasis added).)

> In a specific embodiment, performing the enhanced read operation includes receiving a second address from the corresponding plurality of input/output pins, receiving a second performance enhancement indicator and determining whether an enhanced read operation is to be performed based on *at least information associated with the second performance enhancement indicator.*

(*Id.* at 2:4-11 (emphasis added).)

> In an embodiment, the method also includes determining whether a second enhanced read operation is to be performed based *on at least information associated with the second performance enhancement indicator.*

(*Id.* at 2:14-17 (emphasis added).)

> In Process 350, the performance enhancement indicator is processed to determine whether an enhanced read operation is to be performed based on *at least information associated with the performance enhancement indicator.*

(*Id.* at 10:1-21 (emphasis added); *see also id.* at 10:62-65, 11:17-20.)

As set forth above, the specification makes clear in several places that the determination of whether to perform an enhanced read operation may be based on information other than the performance enhancement indicator. Thus, I find the specification specifically contemplates that a performance enhancement indicator need not, by itself, actually initiate an enhanced read operation. Neither Respondents nor the Staff provides me any sound reason to ignore these explicit teachings from the specification.

Respondents assert in reply that according to Macronix, the performance enhancement indicator could be purely passive information that has no role in determining whether to perform an enhanced read operation. Not true. Under Macronix's proposed construction, the performance enhancement indicator definitely plays a role in determining whether to perform an enhanced read operation, it just may not be the definitive role Respondents and the Staff are pushing for in their proposed constructions.

Respondents argue that the patent applicants underscored in response to a prior art rejection from the PTO during patent prosecution that the performance enhancement indicator causes the chip to enter an enhanced read operation, but Respondents make no effort either in their initial brief or reply to develop that argument. Respondents merely state a conclusion and then cite to a page in the prosecution history leaving it to me to make their argument for them. Having reviewed the portion of the prosecution history to which I was directed I do not find any statement made by the patent applicants that would support Respondents' argument. Accordingly, I find Respondents' argument based on the prosecution history not persuasive.

As discussed above, I find the Macronix's proposed construction more closely aligns with the language of the claims as read in light of the specification and thus find that one of ordinary skill in the art at the time of the invention would construe the term "performance enhancement indicator" to mean "a signal indicating an enhanced read operation is to be performed."

2. "enhanced read operation"

Respondents identified "enhanced read operation" as a term that requires construction. This term appears in claims 1–3 and 9–11 of the '330 patent. The parties have each proposed the following constructions:

Complainants	Respondents	Staff
"read operation in which multiple reads are performed requiring only one read command"	"a read operation with reduced data access time"	"read operation in which multiple reads are performed requiring only one read command"

The Staff originally proposed a construction markedly different from that proposed by Macronix and Respondents, but after thinking it over adopted Macronix's construction. (SMIB at 32.) Basically, the Staff contends Macronix's proposed construction captures the concept of the enhanced read operation described in the specification. (*Id.*) Noting that the term is neither defined in the specification or a dictionary, the Staff does contend the specification provides useful guidance. (*Id.*)

The enhanced read operation "is carried out without requiring a new read command." ('330 patent at 10:49-50.) Later, the patent states that the "single read command allows multiple random data read operations." (*Id.* at 11:28-29.) Moreover, the specification also discloses that "there can be many alternatives, modifications, and variations" to the disclosed embodiments of selected components, pin configurations, and timing sequences for carrying out enhanced read operations.

The Staff contends a POSITA would agree that the common baseline that defines the enhanced read operation within the scope of the '330 patent is a "read operation in which multiple reads are performed requiring on y one read command." (SMIB at 33.) Respondents disagree. (RMIB at 50-54.)

Respondents the purpose of the invention is to allow faster data transfer rates. (RMIB at 50, citing Patent at 1:20-12; 1:44-46; and 6:57-59.) Respondents allege the specification recites three exemplary ways for the "enhanced read operation" of the invention can be implemented to result in faster transfer rates (reduced data access time):

> [First mode] High data transmission rate data read operations using conventional serial peripheral interface pin-out;
>
> [Second mode] Multiple random read operations requiring only one read command; and
>
> [Third mode] Multiple random read operations within a page of data requiring only one read command and partial address information.

(*Id.*) Respondents note these three modes are examples and describe other possible embodiments. (RMIB at 50-52.) Then, Respondents make an interesting statement, which is:

> The construction of "enhanced read operation" must be broad enough to cover all contemplated enhanced read operation modes (including the three that are disclosed and the various combinations of these modes). *Hill-Rom Servs.*, 755 F.3d at 1379 (quoting *Vitronics*, 90 F.3d at 1583 (stating that a construction that excludes preferred embodiments "is rarely, if ever, correct and would require highly persuasive evidentiary support."); *see also Primos, Inc. v. Hunter's Specialties, Inc.*, 451 F.3d 841, 848 (Fed. Cir. 2006) ("While we are mindful that we cannot import limitations from the preferred embodiments into the claim, we also should not normally interpret a claim term to exclude a preferred embodiment.").

(RMIB at 52.) Respondents then aver construction of the "enhanced read operation" must be broad enough to include the embodiments in dependent claims 2, 3, and 10. (*Id.*) This leads to Respondents averment that:

> Macronix's proposed construction limits the scope of claim 1 to only the second mode described above. Thus, it does not encompass the explicit definition of "enhanced read operation" of claims 2 (and 10, which depends from 9) and would exclude the first and third modes above. For this reason, it must be rejected. *See id.*

(RMIB at 53.)

The Staff counters Respondents contentions by noting the logic behind Respondents' declaration that there is problematic because it is unclear [and unstated] what "explicit definition" Respondents can be referring to, since if the term at issue were defined there would be no need to construe it. (SMIB at 33.) Respondents are also claiming Macronix is wrong for not incorporating limitations from the specification into the claim construction. This too is problematic, for what Respondents are seeking to do there is to import specification limitations into claims, which to put it mildly is problematic. *Phillips*, 415 F.3d at 1323; *Kara Tech.*, 582 F.3d at 1348. Basically, the claim does not need to be as broad as matters discussed in a specification, for the applicant can choose to claim less.

Macronix first challenges Respondents' construction because there is nothing in the claims, the specification, or the prosecution history that ties data access tie reduction to the enhanced read operation. (CMIB at 63.) Macronix goes on to point out that "even worse," Respondents' construction introduces the concept of "reduced" time without providing a benchmark or a reference by which to create a comparison. (*Id.*) Macronix contrasts Respondents' method of deriving a construction with its own, *i.e.*, it alleges its construction tracks the fundamental concept of the enhanced read operation described in the specification, which is the ability to perform multiple read operations in sequence without having to send multiple read commands. (*Id.*)

I note the term "enhanced read operation" appears in claims 1, 3, 8, 9, and 11. Claim 1 follows, with the term highlighted to show the context within the overall claim:

> 1. A method for conducting a read operation in an integrated circuit, the method comprising:
>
> receiving a read command;
>
> receiving a first address in a clock cycle after receiving the read command;

> receiving a first performance enhancement indicator in a clock cycle immediately after receiving the first address while before starting to send data out, for determining whether an **enhanced read operation** is to be performed; and
>
> performing the **enhanced read operation**, in case of determining that the **enhanced read operation** is to be performed.

(Claim 1 at 14:25-37.)

Keeping in mind that claim terms must be construed as a whole in light of all of the limitations, I note the plain language is not that difficult to understand. *See Lexion Med., LLC v. Northgate Techs., Inc.*, 641 F.3d 1352, 1356 (Fed. Cir. 2011) ("This Court prefers a claim interpretation that harmonizes the various elements of the claim to define a workable invention."). This is because the "claims themselves provide substantial guidance as to the meaning of particular claim terms [and] the context in which a term is used in the asserted claim can be highly instructive." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*).

Here, as Macronix argues (CMIB at 64), it seems obvious to me the plain language supports Macronix's proposed construction because it connects the determination of whether to perform an "enhanced read operation" to the "performance enhancement indicator" and not to any additional read command. Specifically, claims 1 and 9 recite receiving a first "read command." (Claim 1 at 14:2;, claim 9 at 15:10.) These claims also recite subsequently receiving a "first performance enhancement indicator." (Claim 1 at 14:30-32;., claim 9 at 15:14-16.] The "performance enhancement indicator" is used "for determining whether an enhanced read operation is to be performed." (Claim 1 at 14:30-34; claim 9 at 15:16-18.) Further, claims 3 and 11, both dependent on claims 1 and 9, respectively, provide that the "second performance enhancement indicator" is used "for determining whether the enhanced read operation is to be performed." (Claim 3 at 14:46-48; claim 11 at 16:7-10.) Other than the initial read command recited in the independent claims, the claims do not recite additional read commands.

The specification consistently discloses that the enhanced read operation is a read operation that is performed without the need for additional read commands. (*See, e.g.*, '330 patent at 10:49-50 ("In an embodiment of the enhance read, a data read is carried out without requiring a new read command."), 11:28-29 ("According the embodiment discussed above, the method for enhanced read continues as required by the performance enhance indicator. Thus, a single read command allows multiple random data read operations.").)

The specification also dependably describes that the performance of the "enhanced read operation" involves receiving an additional read address, an additional performance enhancement indicator (for determining whether to perform an additional enhanced read operation after the current enhanced read operation is performed), and outputting data associated with that additional read address. No additional read command is disclosed as being a part of the "enhanced read operation." For example:

> In a specific embodiment, *performing the enhanced read operation includes receiving a second address from the corresponding plurality of input/output pins, receiving a second performance enhancement indicator and determining whether an enhanced read operation is to be performed based on at least information associated with the second performance enhancement indicator*, and waiting n clock cycles, where n is an integer, then outputting data in the integrated circuit using the plurality of input/output pins, the data being associated with the second read address.

('330 patent at 2:4-14.) (emphasis added) Macronix, in fairly exhaustive detail, goes on to cite further excerpts from the specification consistent with the foregoing, as follows:

> In a specific embodiment, the one or more components for performing the enhanced read operation comprise one or more components for performing the following functions:
>
> 1. **receiving a second address** from the plurality of input/output pins;
>
> 2. **receiving a second performance enhancement indicator**; and

3. waiting n clock cycles, where n is an integer, then **outputting data in the memory array in the integrated circuit using the plurality of input/output pins, the data being associated with the second read address.**

[*Id.*, 3:23-33 (emphasis added).]

In a specific embodiment, the method for enhanced read includes the following processes (Fig. 5).

1. (Process 510) **Receiving a second address**;

2. (Process 530) **Receiving a second performance enhancement indicator**;

3. (Process 540) Wait n clock cycles, where n is an integer, then **outputting data in the memory array in the integrated circuit using the plurality of input/output pins concurrently**; and

4. (Process 550) **Determining whether a second enhanced read operation is to be performed based on at least information associated with the second performance enhancement indicator.**

[*Id.*, 10:53-65 (emphasis added); *see also id.*, 4:6-20, 4:59-5:12, 5:49-67, 10:66-11:25, 12:8-27, 13:37-55, Figs. 4B, 5, and 6B.]

Moreover, the specification consistently describes that the determination of whether to perform an enhanced read operation is based on information associated with the first and subsequent performance enhancement indicators and not an additional read command. For example:
As shown, the method uses a combination of processes including a way of transmitting address and data information using a plurality of pins concurrently, and **performing multiple data read operations in response to performance enhance indicator information.**

[*Id.*, 9:1-5 (emphasis added).]

According to a specific embodiment, the invention provides a method for reading data in an integrated circuit. The method includes receiving a read command, which is associated with an enhanced data read, and receiving a first address from a plurality of input/output pins. The method includes **receiving a first performance enhancement indicator and determining whether an enhanced read operation is to be performed based on at least information associated with the first performance enhancement indicator.** The method includes waiting n clock cycles, where n is an integer, then outputting data from a memory array in the integrated circuit using the plurality of input/output pins concurrently. The data is associated with the first read address. The method also includes **performing an enhanced read operation, if it is determined that the enhanced read operation is to be performed based on at least information associated with the performance enhancement indicator.**

[*Id.*, 1:55-2:3 (emphasis added); *see also id.*, 2:39-55, 3:4-22, 3:52-4:5, 4:42-59, 5:23-44, 10:18-21, Figs. 3-6B.]

In a specific embodiment, **performing the enhanced read operation includes** receiving a second address from the corresponding plurality of input/output pins, receiving a second performance enhancement indicator and **determining whether an enhanced read operation is to be performed based on at least information associated with the second performance enhancement indicator**, and waiting n clock cycles, where n is an integer, then outputting data in the integrated circuit using the plurality of input/output pins, the data being associated with the second read address.

[*Id.*, 2:4-14; *see also id.*, 2:56-65, 3:34-38 (emphasis added).]

In a specific embodiment, the method also includes **determining whether a second enhanced read operation is to be performed based on at least information associated with the second performance enhancement indicator.**

[*Id.*, 4:17-20, 5:45-49 (emphasis added).] Indeed, because the performance of the enhanced read operation is tied to the performance enhancement indicator, the '330 patent specification discloses that "the enhanced read is continued as long as the performance enhancement indicator is set." [*Id.*, 13:4-6; *see also id.*, 11:26-28 ("According to the embodiment discussed above, the **method for enhanced read continues as required by the performance enhance indicator.**") (emphasis added).]

(CMIB at 65-67.) Nowhere in any of the text cited by Macronix or the patent specification reviewed by me, is there any association with the disputed term with reducing data access time. Instead, the association is with avoiding further read commands. And, while this may have the effect of reducing data access read time, this is not what these claims are about.

Basically, I find that Respondents seek to expand the scope of the claims by asserting that any read operation in which the data access time is reduced qualifies as an enhanced read operation. Even though the enhanced read operation may have the effect of reducing the time necessary to read any given amount of data, a definition based solely on time is not supported by the intrinsic evidence. Further, as the Staff points out, "By merely requiring reduced access time, it opens the door to encompassing an enhanced read operation that reduces the data access time

simply by increasing the processing speed." (SMIB at 33.) Regardless, the '330 specification of establishes certain metes and bounds on how to perform the enhanced read operation is performed and hence the enhanced read operation of the patent should not be broadly defined on the basis of a time parameter not discussed in the specification.

I note Respondents also cite the prosecution history to support their proposed construction. In an Office Action, the Examiner discussed two types of addressing of memory, burst mode and open-row access wherein he stated that "[b]oth accessing mode [sic] improves [sic] or reduce the access time (e.g., enhances memory read operation)." (Exhibit 5 at MX-ITC-0000948.) Respondents contend the examiners statement is "consistent with the Examiner's understanding of 'enhanced read operation.'" (RMIB at 53.) In my view this is an unsupported allegation, one that is only tangentially related to the issue at hand. As the Staff accurately notes, the comment is grammatically challenging and cannot qualify as the Examiner's understanding of the term at issue, for at best, it seems the Examiner is referring to two modes that may improve or reduce the access times as examples of enhanced memory read operations, without any suggestion that improvement or reduction in access time by itself is sufficient to create an enhanced read operation. Thus, I find the Examiner's statement does not does not stand as a definition or a fair characterization of the Examiner's full understanding of the term.

Based upon the foregoing, I adopt Macronix's construction that an "enhanced read operation" is a "read operation in which multiple reads are performed requiring only one read command."

VIII. CONCLUSION

I find that the disputed terms of the asserted patents shall be construed as follows:

- The term "extend[ing] substantially" requires no construction and shall be construed to have its plain and ordinary meaning as discussed on pages 14-15 of this Order.
- The term "the substrate is coupled to an eternal reference supply applying a ground potential and a positive supply potential" shall be construed as "the substrate is coupled to an external voltage source configured to apply a ground potential and a positive supply potential."
- The term "the integrated circuit further including only a supply pin and a ground pin for supplying power to an integrated circuit" requires no construction and shall be construed to have is plain and ordinary meaning.
- The terms "control inputs," address inputs," and data input/outputs," should require no construction and shall be construed to have their plain and ordinary meaning, but to the extent there is any doubt, I adopt the explanatory construction advocated by the Staff and Macronix, *i.e.*, "pins on an integrated circuit for receiving control signals", "pins on an integrated circuit for receiving address signals", and "pins on an integrated circuit for transferring data into or out of a memory array" respectively.
- The term "sector lock signal" shall be construed to mean "a signal indicating a protected status for a sector in the array."
- The term "set of control signals" requires no construction and shall be construed to have its plain and ordinary meaning.

- The term "transmit[ting] the instruction, the address or the read out data" requires no construction and shall be construed to have its plain and ordinary meaning.
- The term "performance enhancement indicator" shall be construed to mean "a signal indicating an enhanced read operation is to be performed."
- The term "enhanced read operation" shall be construed to mean a "read operation in which multiple reads are performed requiring only one read command."

SO ORDERED.

Thomas B. Pender
Administrative Law Judge

IN THE MATTER OF CERTAIN DEVICES CONTAINING, NON-VOLATILE MEMORY AND PRODUCTS CONTAINING SAME **337-TA-922**

CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **PUBLIC ORDER NO. 10** has been served upon the **Commission Investigative Attorney, Brian Koo, Esq.,** and the following parties as indicated on January 15 2015.

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