PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN GRAPHICS PROCESSORS AND PRODUCTS CONTAINING THE SAME**	**Inv. No. 337-TA-1099**

ORDER NO. 26: GRANTING-IN-PART COMPLAINANT ZIILABS, INC.'S MOTION TO COMPEL

(October 4, 2018)

I. Introduction

On September 13, 2018, Complainant ZiiLabs Inc., Ltd. ("ZiiLabs") moved (1099-021) to compel: (1) Respondent NVIDIA Corporation ("NVIDIA") to produce various categories of source code; and (2) Respondents ASUSTeK Computer Inc., ASUS Computer International, EVGA Corporation, Gigabyte Technology Co., Ltd., G.B.T. Inc., Micro-Star International Co., Ltd., MSI Computer Corp., PNY Technologies Inc., Zotac International (MCO) Ltd., and Zotac USA Inc. ("Respondents") to provide supplemental responses and witness designations to their respective Notices of Deposition. On September 26, 2018, NVIDIA and the Respondents moved (1099-025) for leave to file their opposition to ZiiLabs' motion out of time. NVIDIA and Respondents explain:

> Respondents' Motion and all exhibits except for Exhibit 8, were timely filed on EDIS Monday September 24, 2018 at 5:14 p.m. Due to a technical error while preparing the exhibit for filing, Exhibit 8 was filed on EDIS Monday September 24, 2018 at 5:51 p.m. The Opposition to the Motion to Compel, Exhibits 1 through 31, including Exhibit 8, were served on ZiiLabs, the other Respondents in the Investigation, and the Administrative Law Judge's Attorney Advisor by 5:43 p.m. that evening.

(Mot. at 1.) The motion represents "[a]ll parties have indicated that they do not oppose [the motion for leave]." (*Id.* at 2.) Also on September 26, 2018, NVIDIA and Respondents filed their underlying

opposition. For the reasons stated therein, and in light of the motion's non-opposition, NVIDIA and Respondents' motion for leave (1099-025) is hereby granted.

II. ZiiLabs' Motion

ZiiLabs specifically seeks an order requiring NVIDIA to "provide production of source code as detailed in S. Datta's letter dated August 21, 2018, to Nvidia, which pertains to the structure and function of Nvidia's Products accused of infringement in this Investigation." (Mot. Mem. at 1.) ZiiLabs contends NVIDIA "produces source code in bits and pieces, forcing ZiiLabs to review and analyze the code in order to determine that the deficiencies it previously raised still exist" in addition to producing that code in proprietary languages in place of "commonly understood hardware languages such as Verilog RTL." (*Id.* at 1-2.) ZiiLabs identifies thirteen categories of production it moves to compel NVIDIA to produce.

1) Verilog RTL generated during the build process

For this category, ZiiLabs seeks "the equivalent Verilog RTL files for Fermi, Kepler, Maxwell, Volta, and Turing that Nvidia has already produced with respect to Pascal [architecture] in the Verilog RTL format, along with the outstanding deficiencies identified in items 2-11 in the August 21, 2018 letter." (*Id.* at 8.) ZiiLabs contends these materials have only been produced in NVIDIA's proprietary [ ] files. (*Id.*) ZiiLabs argues it is in compliance with a prior agreement between the parties that Verilog RTL files for the Pascal architecture would be produced for ZiiLabs to review, and then, upon review, ZiiLabs would make a "targeted identification" of important files for NVIDIA to collect for the other architectures. (*Id.*) ZiiLabs claims that NVIDIA began this process with just a subset of Pascal Verilog RTL files, instead of the "entire archived build chip code," so that ZiiLabs request for the same code for the other architectures is already "targeted" in the manner contemplated by the Parties. (*Id.*) ZiiLabs argues "[t]he requested Verilog RTL code is relevant, because Verilog

RTL is a well-known universal hardware language for which standard source code review tools can be used" as opposed to NVIDIA's proprietary [ ] language. (*Id.* at 9.)

2) Source code showing instantiation of produced source code modules

For this category, ZiiLabs seeks "specific missing Verilog modules" that "show which modules produced to date are used in the chip and how the modules are interconnected, *e.g.*, to service a cache miss or perform rasterization, as described by the asserted claims." (*Id.*) ZiiLabs argues certain [ ] do not provide the same information in readily understandable manner. (*Id.* at 9-10.)

3) [ ] file(s)

For this category, ZiiLabs seeks a certain [ ] for the Pascal GP10B GPU, but notes it is willing to withdraw the request if certain stipulations are made by NVIDIA. (*Id.* at 10.)

4) [ ] directories

For this category, ZiiLabs seeks [ ] directions for the Fermi, Kepler, Maxwell, Pascal, Volta, and Turing architectures, including[ ] (*Id.*) ZiiLabs disputes NVIDIA's representation that such code was already produced. (*Id.*)

5) Driver code for each architecture

For this category, ZiiLabs seeks "driver code for the Fermi, Kepler, Maxwell, Pascal, Volta, and Turing architectures." (*Id.* at 11.) ZiiLabs disputes NIVIDIA's contention that ZiiLabs only recently requested this category of code. (*Id.* (citing Mot., Exs. B, R, S).)

6) Verilog RTL files that connect produced modules to each other

For this category, ZiiLabs seeks "Verilog RTL files that connect each of the produced modules to each other, for the Fermi, Kepler, Maxwell, Pascal, Volta, and Turing architectures." (*Id.*) ZiiLabs argues that NVIDIA's offer to meet and confer on September 14, 2018 was "not proper and counterproductive at this stage of discovery" (*id.*) and that ZiiLabs should not have the burden to

identify files with specificity, as NVIDIA contended on September 10, 2018 (*id.* at 12 (citing Mot., Ex. K)).

7) Modules showing connection of clock signals from the top-level module

For this category, ZiiLabs seeks a variety of Verilog RTL source code showing the connection of clock signals between modules. (*Id.*) ZiiLabs argues this code is relevant to "physically synchronous" claim limitations in the '156 patent. (*Id.* at 12-13.) ZiiLabs argues that NVIDIA's offer to meet and confer on this category is again "not proper and counterproductive at this stage of discovery." (*Id.* at 13)

8) Pascal (GP10B) directories and files

For this category, ZiiLabs seeks "missing Pascal (GP10B) directories and files, including any corresponding Fermi, Kepler, Maxwell, Volta, and Turing files." (*Id.*) ZiiLabs argues NVIDIA's prior promise to search for and produce the code has not resulted in any production. (*Id.*)

9) Specific files for Fermi, Kepler, Maxwell, Pascal, Volta, and Turing GPU architectures

For this category, ZiiLabs seeks additional "specific, missing files for the Fermi, Kepler, Maxwell, Pascal, Volta, and Turing files," and identifies several in particular to which NVIDIA has made promises of searching but not made any production for. (*See id.* at 13-14.)

10) [ ] files

For this category, ZiiLabs seeks "missing [ ] files, including at least the [ ] and [ ] files, for the Fermi, Kepler, Maxwell, Pascal, Volta, and Turing architectures." (*Id.* at 14.) ZiiLabs argues that NVIDIA failed to give a response on whether this category would be produced; instead improperly asking ZiiLabs to explain the basis for requesting the code. (*Id.*)

11) Multiple versions of Turing code

For this category, ZiiLabs seeks "top-level Verilog files for specific modules and an indication as to which of multiple versions of produced Turing architecture source code is used during RTL synthesis for the actual GPU manufactured." (*Id.*) ZiiLabs notes that categories 1 and 2, above, encompass this request. (*Id.* at 15.)

12) Commercial name for GP10B

For this category, ZiiLabs explains the dispute has been resolved. (*Id.*)

13) Verilog RTL for each GPU in NVIDIA's G.R. 7.2 disclosure

For this category, ZiiLabs seeks "the relevant, standard Verilog RTL (*e.g.*, .v or .sv files) that was generated and used during RTL synthesis for each of the GPUs identified in Nvidia's Ground Rule 7.2 Disclosure, including all of the files identified in items 1-11 above." (*Id.*)

In addition to these source code issues, ZiiLabs also seeks an order requiring the Respondents to respond and provide witnesses to Notices of Deposition. (*Id.* at 1.) ZiiLabs explains that the parties explored the possibility of using stipulations and other discovery in place of the depositions, but that no progress has been made. (*See id.* at 16-18.) Specifically, ZiiLabs alleges "Respondents began supplementing discovery responses on September 11, 2018, but did not provide any supplements to the Notices. Respondents sent an email on September 11, 2018, stating that the parties are not at an impasse regarding the depositions of Asus, EVGA, Gigabyte, MSI, PNY, and Zotac because Respondents are willing to agree to various stipulations and document productions." (*Id.* at 18 (citing Mot., Ex. M).) ZiiLabs continues, "Respondents have not raised any argument that the requested discovery is not relevant to the Investigation. . . . Regardless, Respondents have not signed the stipulations or produced the requested discovery." (*Id.* at 19.)

III. Respondents' Opposition

On source code issues, NVIDIA argues the motion should be denied for two reasons: "[f]irst, it violates the Ground Rules and is thus procedurally improper;" and "[s]econd, it seeks discovery that is irrelevant and/or duplicative and therefore has no bearing on any issue in this Investigation." (Opp. at 9.)

Regarding procedure, NVIDIA specifically contends "the majority of the complaints in Complainant's August 21, 2018 letter were brand new and had never been discussed during the parties' prior discovery committee meetings or meet-and-confers," and following this letter, "NIVIDIA investigated Complainant's new requests, agreed to supplement its source code production in response to reasonably supplemental requests, and offered to meet and confer regarding the scope and relevance of the remaining requests" through a communication on September 10, 2018. (*See id.* at 10 (referring to Mot., Ex. K).) NVIDIA claims that ZiiLabs opted not to respond to NVIDIA's response and instead filed the present motion, which evidences ZiiLabs lack of "intensive good faith effort to resolve the discovery dispute" under Ground Rules 5.1.2 and 5.4.1. (*Id.* at 10-12.) NVIDIA notes that since the filing of the present motion, it: produced supplemental source code for topics 5, 6, 8, 9, 10, and 11; repeated its position that it already produced the code requested in items 3 and 4; offered to discuss the scope of the remaining requests. (*Id.* at 11.) NVIDIA suggests these offers alone is sufficient to deny ZiiLabs' motion. (*Id.* (citing *Certain Mobile Devices, Associated Software and Components Thereof*, Inv. No. 337-TA-744, Order No. 11 (July 12, 2011)); *see id.* at 12.)

Regarding source code, NVIDIA specifically contends "each and every category has either been produced, will be produced, or is irrelevant/duplicative." (*Id.* at 12.)

1) Verilog RTL generated during the build process

NVIDIA opposes production of this category because "[

]" (*Id.* at 13.)

Rather, according to NVIDIA, "[

]" (*Id.* at 14 (citations omitted).) NVIDIA claims, as such, it is not

[

]." (*Id.* at 15 (citation omitted).) NVIDIA thus views this category as duplicative of what has already been produce. (*Id.*) NVIDIA claims that any proprietary language difficulties ZiiLabs encountered with the produced code should have been resolvable with "produced documentation describing the syntax and structure of that code, including tutorials, reference manuals, and similar instructional documents." (*Id.* at 16 (citations omitted).) NVIDIA concludes "[t]he fact that Complainant believes reviewing the automatically generated 'standard Verilog RTL' would be easier and less time-consuming does not justify compelling NVIDIA to produce the duplicative and irrelevant code." (*Id.* (citation omitted).)

NVIDIA also opposes production of this category because ZiiLabs' request contradicts ZiiLabs' prior agreement to review the Pascal Verilog RTL code and then only request *subsets of that code* ("targeted identification") for other architectures. (*Id.* at 17 (citing Opp., Ex. 14; Mot., Ex. A).)

2) Source code showing instantiation of produced source code modules

NVIDIA opposes production of this category because it relates to modules that have "nothing to do with Complainant's infringement contentions" and do not show functionality but how other modules are interconnected. (*Id.* at 18 (citing Mot. at 9, Mot., Ex. A).) NVIDIA adds that "[t]here is not a single claim limitation that relates to 'instantiation' of the accused GPUs or that even might remotely be needed to prove alleged infringement." (*Id.*) NVIDIA claims these files

have "zero value" (*id.* at 18) and will not show what ZiiLabs wants them to show—which modules produced to date are used in which chip (*id.* at 19 (citing Mot. at 9)). NVIDIA adds that other source code—[ ]—produced in June shows "interconnection between relevant modules" if that is what ZiiLabs wants. (*Id.* (citing Opp., Exs. 10, 11).) NVIDIA adds "Complainant has yet to identify *any* information that it cannot locate in the already produced source code that it contends might reside in the 'instantiation' files." (*Id.* at 20.)

3) [ ] file(s)

NVIDIA opposes production of this category because it has allegedly already been produced. (*Id.* at 20.) NVIDIA suggests ZiiLabs actually wants NVIDIA to "reproduce [ ] in its production of 'standard Verilog RTL' for Pascal." (*Id.* (citing Opp., Exs. 10, 11).) NVIDIA says this is impossible as the file "does not exist in that format." (*Id.*) NVIDIA adds that, to the extent ZiiLabs wants it, the [ ] files for the GP10B GPU need not be produced because NVIDIA has already admitted "no material difference [exists] between the source code for different GPU product families that use the same GPU architecture." (*Id.* at 21 (citing Opp., Ex. 22).)

4) [ ] directories

NVIDIA opposes production of this category because it is undisputed that "top-level [ ]" were produced in June and what remains is a general concern from ZiiLabs that files might be missing. (*Id.* at 21 (citing Mot., Ex. G; Opp, Ex. 10).) NVIDIA asserts it is "willing to produce other relevant [ ] folders, but it cannot do so until Complainant adequately identifies the folders or files." (*Id.*) Thus, NVIDIA views this category as a clear fishing expedition. (*Id.*)

5) Driver code for each architecture

NVIDIA opposes production of this category as moot. (*Id.* at 22.) Specifically, NVIDIA claims "[a]s of the date of this opposition brief, NVIDIA has produced relevant driver code for each architecture." (*Id.* (citing Opp., Ex. 23).) Rather, according to NVIDIA, it "has produced the source code for the accused features and functionalities in the accused architectures as well as the relevant 'interconnection' files." (*Id.*)

6) Verilog RTL files that connect produced modules to each other

NVIDIA opposes production of this category because it cannot discern what Complainant seeks. (*Id.*) For the particular [ ] module noted in ZiiLabs' motion and August 21 letter, NVIDIA represents its source code and "standard RTL Verilog" has since been produced. (*Id.* at 22, n.10.) NVIDIA notes it "offered to meet and confer to determine the identity of the alleged 'missing' modules and collect relevant code if it exist[s]." (*Id.* at 23.)

7) Modules showing connection of clock signals from the top-level module

NVIDIA opposes production of this category because it "potentially encompasses the entire source code for each accused architecture" and is thus overbroad and burdensome. (*Id.*) NVIDIA claims it has already "produced the entire source code repository (including Pascal standard Verilog RTL) for the Streaming Multiprocessor, which includes all clock signals that connect to each component within the Streaming Multiprocessor." (*Id.* (citing Opp., Ex. 10).) Nevertheless, NVIDIA states clearly, "if Complainant is requesting source code describing clock signals *outside* of the Streaming Multiprocessor, that does not relate to any issue in this Investigation, and Complainant has failed to show at any point it is entitled to discovery of that information." (*Id.* (citation omitted).)

8) Pascal (GP10B) directories and files

NVIDIA states this category is moot because "NVIDIA has produced the specific files that Complainant requested and thereby resolved this dispute." (*Id.* at 24.)

9) Specific files for Fermi, Kepler, Maxwell, Pascal, Volta, and Turing GPU architectures

For this category, NVIDIA states the specific [ ] file has been produced, thus resolving this dispute. (*Id.*) NVIDIA likewise believes there is no longer a dispute over "project variables" after it produced "files that provide parameters definitions." (*Id.*) For [ ] command line inputs," NVIDIA explains this category is not code but commands entered by engineer for debugging or testing—and thus there is nothing to produce. (*Id.* at 25.)

10) [ ] configuration files

NVIDIA states this category is moot because "NVIDIA has agreed to collect and produce these files." (*Id.* at 24.)

11) Multiple versions of Turing code

NVIDIA states this category is moot because "NVIDIA has agreed to identify how the produced source code folders are used in the Turing GPUs." (*Id.* at 25.)

12) Commercial name for GP10B

NVIDIA states this dispute has been resolved as in ZiiLabs' motion.

13) Verilog RTL for each GPU in NVIDIA's G.R. 7.2 disclosure

NVIDIA opposes production of this category because "[u]nlike Item No. 1, which requests the 'standard Verilog RTL' for each accused *architecture*, Item No. 13 requests Verilog RTL for *each individual GPU*, an exponential increase from Item No. 1." (*Id.* at 26.) NVIDIA continues, "NVIDIA already has represented in its requests for admission that it has discerned no differences relevant to Complainant's infringement theories between the source code for different chips that use the same

GPU architecture." (*Id.* (citing Opp., Ex. 22 at RFAs 106-110).) Thus, according to NVIDIA, this is completely duplicative and burdensome information to collect. (*Id.*)

Regarding depositions, Respondents contend the motion should be denied because "the parties have never been at an impasse concerning depositions of ASUS, EVGA, Gigabyte, MSI, PNY, and Zotac." (*Id.* at 27.) Rather, according to Respondents:

> Throughout fact discovery, the parties have operated under the assumption that these depositions would not be necessary if the Respondents enter into stipulations and provide written discovery on certain issues including importation and modification of software that Respondents get from NVIDIA. Respondents have worked diligently to enter these agreements, but Complainant has repeatedly delayed or changed its position about what is necessary to resolve the need for depositions. Given the uncertainty of Complainant's ever-changing requests, Respondents told Complainant that they would put up witnesses for deposition to the extent any issues remain outstanding. Complainant simply needs to make up its mind about whether it wants to take the depositions. But a motion to compel them is completely unnecessary.

(*Id.*) More specifically, Respondents claim they "agreed to provide the requested 'technical' information via interrogatory response" and did so on September 23, 2018. (*Id.* at 30.) Respondents claims this resolves the dispute as concerns Topics 1-14 and 52 as in the Notices of Deposition at issue. (*Id.*) For the "use" topics, Respondents state they have "agreed to 'provide a witness on these topics subject to our objections.'" (*Id.* (citing Opp., Ex. 27).) Regarding affirmative defense topics, Respondents claim they are not pursuing "unique affirmative defenses," with the exception that:

> ASUS, Gigabyte, and PNY are pursuing an *EPROMs* defense with respect to certain accused products. For this one exception, the parties have agreed that if ASUS, Gigabyte, and PNY provide information for these products that shows the cost of the GPU relative to the overall product, then it should resolve the need for a deposition. To the extent Complainant disagrees, ASUS, Gigabyte, and PNY have agreed to "provide a witness on these topics subject to our objections." Ex. 27.

(*Id.* at 31.) Respondents thus view this portion of the motion as moot as well.

IV. Analysis

Having reviewed the pleadings, the undersigned finds as follows.

For source code category no. 1, the undersigned finds ZiiLabs has adequately shown the relevance of the requested Verilog RTL files to the claims at issue in this case, and NVIDIA does not meaningfully dispute that relevance. Instead, NVIDIA argues the content of those files is automatically generated and "dictated by" the [ ] source code already produced. (Opp. at 15.) Thus, NIVIDIA reasons "what Complainant seeks is completely duplicative of what NVIDIA produced." (*Id.*) To the contrary, the undersigned finds NVIDIA's assertion that the Verilog RTL files will not "show how the Accused Products actually work" as compared to the produced source code (*id.* at 13) shows that the files are not so duplicative. Similarly, while NVIDIA argues "[t]he fact that Complainant believes reviewing the automatically generated 'standard Verilog RTL' would be easier and less time-consuming does not justify compelling NVIDIA to produce the duplicative and irrelevant code" (*id.* at 16), the undersigned finds the opposite. Such code should be produced exactly because it will facilitate resolution of the issues.

Thus, the issue turns on NVIDIA's burden to collect and produce that code. On this point, NVIDIA argues "Complainant's request is precisely the type of burdensome and duplicative discovery that the discovery rules prohibit" (*id.* at 14) but then fails to explain any details of that burden beyond [

] (*id.* at 15). The undersigned does not find this to be a persuasive explanation of burden under 19 C.F.R. § 210.27(c), (d).[1]

[1] The undersigned declines to evaluate whether or not ZiiLabs or NVIDIA have breached the terms of the intra-party discovery agreement referenced in NVIDIA's opposition.

Thus, ZiiLabs' motion is hereby granted with respect to the Verilog RTL code identified in category no. 1.

For category no. 2, the undersigned finds NVIDIA's argument of irrelevance is undercut by its acknowledgement that the modules show "'how the modules are interconnected.'" (Opp. at 18.) Similar to category no. 1, NVIDIA's insistence that its produced source code and [ ] files more than adequately show the interconnections is not grounds to withhold potentially "easier and less time-consuming" files that show the same. Further, similar to category no. 1, NVIDIA has not addressed the burden involved in collecting these files in dissatisfaction of 19 C.F.R. § 210.27(c).

Thus, ZiiLabs' motion is hereby granted with respect to the Verilog RTL code identified in category no. 2.

For category no. 3, the undersigned finds NVIDIA's reference to its RFA responses (*see* Opp. at 21 (citing Opp., Ex. 22)) likely moots ZiiLabs' request in the manner expected in ZiiLabs' motion (*see* Mot. Mem. at 10). Thus, ZiiLabs' motion is hereby denied as moot with respect to category no. 3.

For category no. 4, the undersigned finds that, despite NVIDIA's assertions of "mystery" (Opp. at 21), ZiiLabs has identified the [ ] and [ ] directories as examples of what it seeks (Mot. Mem. at 10). Thus, ZiiLabs' motion is hereby granted with respect to [ ] and [ ] directories as described in category no. 4.

For category no. 5, the undersigned finds NVIDIA has resolved this dispute based on its representation that "[a]s of the date of this opposition brief, NVIDIA has produced relevant driver code for each architecture." (Opp. at 22.) Thus, ZiiLabs' motion is hereby denied as moot with respect to category no. 5.

For category no. 6, the undersigned finds NVIDIA has largely met its obligation at this time through its representation that it produced the Verilog RTL code for the [ ] module for the

Pascal architecture. (Opp. at 22, n. 9, 10.) To the extent such files exist, the [ ] module, or its equivalent, should also be produced for the other architectures mentioned in ZiiLabs' motion. (*See* Mot. Mem. at 11.) Beyond that, the undersigned agrees with NVIDIA that ZiiLabs must be more specific than "connect each of the produced modules together" in its identification of missing materials. Thus, ZiiLabs' motion is hereby granted-in-part with respect to category no. 6.

For category no. 7, the undersigned finds that, similar to category no. 1 (and perhaps encompassed by it), NVIDIA should produce the equivalent Verilog RTL code for the non-Pascal architectures that it represents it has already produced for the Pascal architecture (*see* Opp. at 23), in addition to those items (a)-(d) referenced in ZiiLabs' motion (Mot. Mem. at 12 (citing Mot., Ex. A at 4)). This limited scope should alleviate NVIDIA's concerns over the burden in producing "the entire source code for each accused architecture" and "clock signals outside of the Streaming Multiprocessor." (Opp. at 23-24.) Thus, ZiiLabs' motion is hereby granted-in-part with respect to category no. 7.

For category no. 8, the undersigned finds NVIDIA has resolved this dispute based on its representation that "NVIDIA has produced the specific files that Complainant requested." (Opp. at 24.) Thus, ZiiLabs' motion is hereby denied as moot with respect to category no. 8.

For category no. 9, the undersigned finds NVIDIA has resolved this dispute with respect to [ ] files based on its representation that "NVIDIA has produced that file." (*Id.*) With respect to the "command line input," the undersigned NVIDIA has adequately explained how there is no source code related to this request as opposed to other forms of discovery. Thus, ZiiLabs' motion is hereby denied with respect to category no. 9.

For category no. 10, the undersigned finds the dispute has or will be most likely resolved as ZiiLabs has identified with specificity what it seeks (Mot. Mem. at 14) and NVIDIA has represented

it "has agreed to collect and produce these files" (Opp. at 25). Thus, ZiiLabs' motion is hereby denied as moot with respect to category no. 10.

For category no. 11, the undersigned finds the dispute has or will be most likely resolved as NVIDIA has represented it "has agreed to identify how the produced source code folders are used in the Turing GPUs." (Opp. at 25.) Further, the undersigned agrees ZiiLabs' request for "top-level Verilog files" is too ambiguous to enforce. Thus, ZiiLabs' motion is hereby denied with respect to category no. 11.

For category no. 12, both parties explain there is no longer a dispute. (Mot. Mem. at 15; Opp. at 25.)

For category no. 13, the undersigned finds NVIDIA's reference to its RFA responses (*see* Opp. at 26 (citing Opp., Ex. 22)) likely moots ZiiLabs' request in the manner expected in ZiiLabs' discovery letter (*see* Mot., Ex. A at 6 ("To the extent Nvidia is willing to provide a stipulation as to the representativeness of the source code produced to date (and also of the source code to be produced in response to this letter) as compared to each of Nvidia's G.R. 7.2 products, ZiiLabs is amenable to mooting this request.")). To the extent it does not, the undersigned finds it is too late to justify the production of all Verilog RTL code for all GPU products (as opposed to each architecture) given what has already been produced or otherwise ordered to be produced in this Order. Thus, ZiiLabs' motion is hereby denied as moot with respect to category no. 13.

With respect to the deposition notices directed to the non-NVIDIA Respondents, the undersigned disagrees with Respondents' central premise that there is no impasse between the parties. (*See* Opp. at 27.) ZiiLabs is entitled to corporate testimony on the relevant topics it has noticed. While Respondents argue they "have never refused to provide the information Complainant is seeking or deposition testimony to the extent necessary" (*id.* at 28) and provided some of the requested "technical" information through interrogatory responses (*id.* at 30), the fact remains that the

Thus, ZiiLabs' motion is hereby granted with respect to the deposition notices. Respondents are ordered to produce witnesses in response to ZiiLabs' deposition notices on or before October 16, 2018. The undersigned understands that with the close of fact discovery having passed on September 28, 2018, ZiiLabs need not file a motion for leave to take these depositions out of time.

Within seven days of the date of this document, the parties shall submit to the Office of the Administrative Law Judges a joint statement as to whether or not they seek to have any portion of this document deleted from the public version. If the parties do seek to have portions of this document deleted from the public version, they must submit to this office a copy of this document with red brackets indicating the portion or portions asserted to contain confidential business information. The submission may be made by email and/or hard copy by the aforementioned date and need not be filed with the Commission Secretary.

SO ORDERED.

Charles E. Bullock
Chief Administrative Law Judge

CERTAIN GRAPHICS PROCESSORS AND PRODUCTS CONTAINING THE SAME

INV. NO. 337-TA-1099

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **Order No. 26** has been served by hand upon the following parties as indicated, on OCT 12 2010.

Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street SW, Room 112A
Washington, DC 20436

FOR COMPLAINANT ZIILABS INC., LTD.	
William D. Belanger, Esq. **PEPPER HAMILTON LLP** 19th Floor, High Street Tower 125 High Street Boston, MA 02110	( ) Via Hand Delivery ( ) Express Delivery (✓) Via First Class Mail ( ) Other: _____
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FOR RESPONDENTS NVIDIA CORPORATION, ASUSTeK COMPUTER INC., ASUS COMPUTER INTERNATIONAL, EVGA CORPORATION, GIGABYTE TECHNOLOGY CO., LTD, G.B.T. INC., MICRO-STAR INTERNATIONAL CO. LTD., MSI COMPUTER CORP., PNY TECHNOLOGIES, INC., ZOTAC INTERNATIONAL (MCO) LTD., ZOTAC USA, INC.	
S. Alex Lasher, Esq. **QUINN EMANUEL URQUHART & SULLIVAN, LLP** 1300 I Street NW Suite 900 Washington, DC 20005	( ) Via Hand Delivery ( ) Express Delivery (✓) Via First Class Mail ( ) Other: _____