

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of

**CERTAIN COMPUTING OR GRAPHICS
SYSTEMS, COMPONENTS THEREOF, AND
VEHICLES CONTAINING SAME**

Inv. No. 337-TA-984

ORDER No. 42: CONSTRUING TERMS OF THE ASSERTED PATENTS

(July 15, 2016)

TABLE OF CONTENTS

	Page
I. PROCEDURAL BACKGROUND	1
II. OVERVIEW OF THE '428 AND '935 PATENTS	4
A. The '428 Patent	4
B. The '935 Patent	6
III. LEGAL STANDARDS	9
IV. THE PERSON OF ORDINARY SKILL IN THE ART	13
A. Legal Standards	13
B. The Computer Graphics Patents ('428, '935, and '945 Patents)	14
C. The Memory Systems Patent ('439 Patent)	15
V. CLAIM CONSTRUCTION OF DISPUTED TERMS	16
A. '428 Patent Disputed Term: "texture address module"	16
1. Parties' Arguments	18
2. Applicability of § 112, ¶ 6	19
3. Construction Analysis	21
B. '935 Patent Disputed Terms	23
1. "arbitration module"	23
2. "operation code"	29
3. "computation engine"	33
4. "in an order to minimize idle time of the computation engine"	36
VI. CONCLUSION	40

TABLE OF ABBREVIATIONS

CIMB	Complainant's Corrected Initial Claim Construction Brief filed May 4, 2016
CRMB	Complainant's Reply Claim Construction Brief filed May 20, 2016
RIMB	Respondents' Initial Claim Construction Brief filed May 4, 2016
RRMB	Respondents' Reply Claim Construction Brief filed May 20, 2016
SMB	Staff's Initial and Reply Claim Construction Brief filed May 12, 2016
Tr.	Transcript

The claim terms construed in this Order are done so for the purposes of this Investigation. Hereafter, discovery and briefing in this Investigation shall be governed by the construction of the claim terms in this Order. Those terms not in dispute need not be construed. *See Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms).

I. PROCEDURAL BACKGROUND

On December 28, 2015, Complainant Advanced Silicon Technologies LLC (“AST”) filed a complaint against Respondents,

Bayerische Motoren Werke AG, BMW of North America, LLC, BMW Manufacturing Co., LLC, Fujitsu Ten Limited, Fujitsu Ten Corp. of America, Inc., Harman International Industries, Inc., Harman Becker Automotive Systems, Inc., Harman Becker Automotive Systems GmbH, Honda Motor Co., Ltd., Honda North America, Inc., American Honda Motor Co., Inc., Honda Engineering North America, Inc., Honda of America Mfg., Inc., Honda Manufacturing of Alabama, LLC, Honda Manufacturing of Indiana, LLC, Honda R&D Americas, Inc., NVIDIA Corporation,¹ Renesas Electronics Corporation, Renesas Electronics America, Inc., Texas Instruments Inc., Toyota Motor Corporation, Toyota Motor North America, Inc., Toyota Motor Sales, U.S.A., Inc., Toyota Motor Engineering & Manufacturing North America, Inc., Toyota Motor Manufacturing, Indiana, Inc., Toyota Motor Manufacturing, Kentucky, Inc., Toyota Motor Manufacturing, Mississippi, Inc., Volkswagen AG, Volkswagen Group of America, Inc., Volkswagen Group of America Chattanooga Operations, LLC, Audi AG, and Audi of America, LLC,

collectively “Respondents,” asserting infringement of U.S. Patent No. 6,339,428 (“the ’428 patent”), U.S. Patent No. 6,546,439 (“the ’439 patent”), U.S. Patent No. 6,630,935 (“the ’935 patent”), and U.S. Patent No. 8,933,945 (“the ’945 patent”).

¹ On April 27, 2016, Complainant AST and Respondent NVIDIA Corporation (“NVIDIA”) reached a settlement agreement and filed a joint motion to terminate NVIDIA from the investigation, which I granted on May 10, 2016. *See* Order No. 33, Inv. No. 337-TA-984 (U.S.I.T.C. May 10, 2016).

By publication of a notice in the Federal Register on February 3, 2016, the U.S.

International Trade Commission ordered that:

Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain computing or graphics systems, components thereof, and vehicles containing same by reason of infringement of one or more of claims 1-6, 8, 9, 10-14, 16, 17, and 25-29 of the '428 patent; claims 1-11 and 14-16 of the '439 patent; claims 1, 2, and 4-8 of the '935 patent; and claims 1-11 and 21 of the '945 patent, and whether an industry in the United States exists or is in the process of being established as required by subsection (a)(2) of section 337.

81 F.R. 5783 (Feb. 3, 2016).

A *Markman* hearing was held in this investigation on Monday, June 20, 2016 and Tuesday, June 21, 2016. Complainant AST and Respondents filed initial claim construction briefs on May 4, 2016, and reply claim construction briefs on May 20, 2016. The Commission Investigative Attorney ("Staff") filed its combined initial and reply claim construction brief on May 12, 2016.

The parties initially selected the following disputed claim terms in their joint identification of claim terms for construction filed April 15, 2016:

No.	Term in Dispute	Claim / Patent
1	texture address module	claims 1 and 10 of the '428 patent
2	requested memory operation buffer	Claims 1, 4, and 14 of the '439 patent
3	arbitration module	claim 1 of the '935 patent
4	operation code	claims 1 and 7 of the '935 patent

No.	Term in Dispute	Claim / Patent
5	application specific prioritization scheme	claim 1 of the '935 patent
6	computation engine	claim 1 of the '935 patent
7	application	claim 1 of the '935 patent
8	in an order to minimize idle time of the computation engine	claim 1 of the '935 patent
9	repeating tile pattern includes a horizontally and vertically repeating pattern of [square] regions	claims 1 and 21 of the '945 patent
10	$N \times M$ number of pixels	claim 21 of the '945 patent

Subsequently, the parties narrowed their disputes and agreed on constructions for the following claim terms:

(1) “requested memory operation buffer” (plain and ordinary meaning) (as indicated in email from Complainant AST’s counsel dated June 14, 2016);

(2) “repeating tile pattern includes a horizontally and vertically repeating pattern of [square] regions” (“repeating tile pattern” means an arrangement of tiles that includes at least two tiles in a row and at least two tiles in a column, and “includes a horizontally and vertically repeating pattern of [square] regions” has a plain and ordinary meaning and need not be construed) (as indicated in email from Complainant AST’s counsel dated June 14, 2016);

(3) “application” (“application” means “a plurality of threads”) (*see* June 20, 2016 *Markman* Tr. at 115:7-10); and

(4) “application specific prioritization scheme” (plain and ordinary meaning) (*see* June 21, 2016 *Markman* Tr. at 262:10-15).

In addition, because Complainant AST moved to terminate the investigation with respect to claim 21 of the '945 patent, the dispute over the term “ $N \times M$ number of pixels” is moot. (Motion Docket No. 984-042.) Thus, only claim terms 1, 3, 4, 6, and 8 remain in dispute and are addressed herein.

II. OVERVIEW OF THE '428 AND '935 PATENTS

A. The '428 Patent

The '428 patent was filed on July 16, 1999 and issued on January 15, 2002, to inventors Mark C. Fowler, Pau Vella, and Michael T. Wright.² The title of the '428 patent is: “Method and Apparatus for Compressed Texture Caching in a Video Graphics System.” The '428 patent relates generally to a method and apparatus for reducing memory bandwidth usage in video graphics texturing operations through the use of compressed texture caching in a video graphics system. *See* '428 patent at 1:6-8, 2:26-28. For example, claim 1 of the '428 patent recites:

A video graphics texture mapping circuit, comprising:

memory storing compressed texture information corresponding to at least one texture;

a cache operably coupled to the memory, wherein the cache stores a portion of the compressed texture information;

a texture address module operably coupled to the memory and the cache, wherein the texture address module determines whether texture data for a texturing operation is stored in the cache, wherein when the texture data is not stored in the cache, the texture address module copies the texture data from the memory to the cache, wherein the texture address module provides control information to the cache such that the cache outputs the texture data; and

² The effective date of the '428 patent pre-dates the America Invents Act (“AIA”) enacted by Congress on September 16, 2011.

a decompression block operably coupled to the cache, wherein the decompression block decompresses the texture data to produce uncompressed texture data for use in the texturing operation.

Figure 1 of the '428 patent, reproduced below, illustrates a video graphics texture mapping circuit according to the invention.

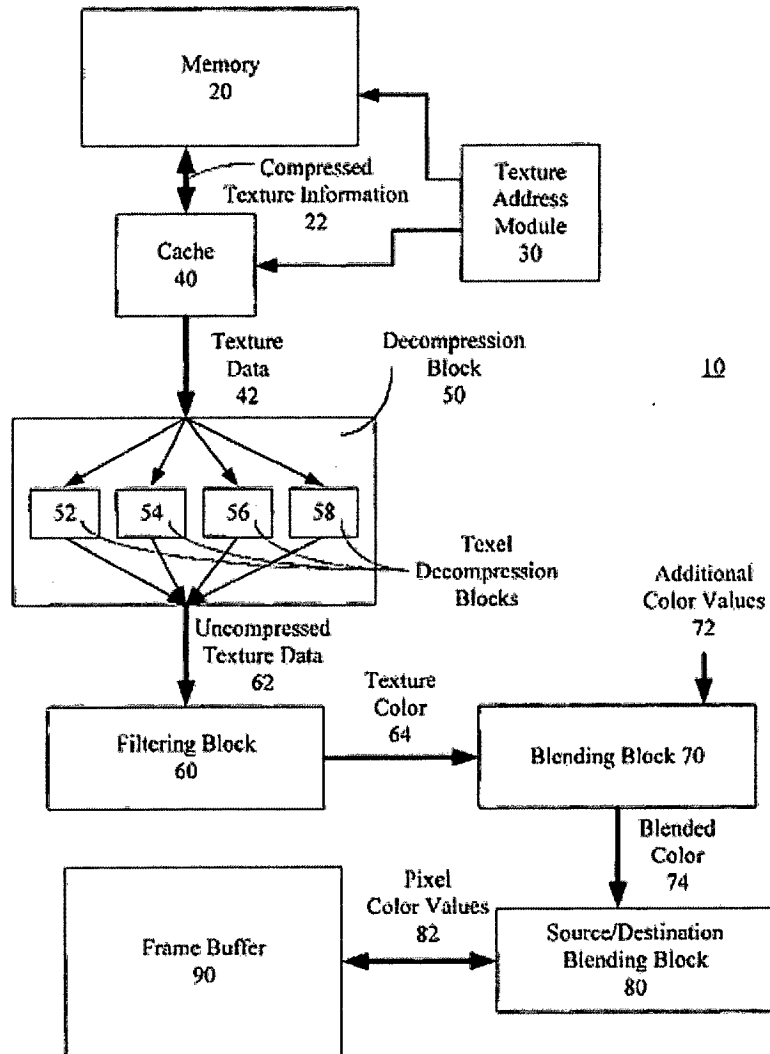


Figure 1.

The '428 patent specification explains:

In order to minimize the memory bandwidth required to fetch the compressed texture information 22 from the memory 20 for usage, the cache 40 is included in the video graphics texture mapping circuit 10. The texture information stored in the cache 40 remains

in the compressed format, thus enabling the cache 40 to effectively store more texture information than it could if the texture information was decompressed prior to storage in the cache 40.

...

[A] texture address module 30 is used to determine whether or not the texture data for a particular texturing operation is currently stored in the cache 40. When the texture data is not stored in the cache 40, the texture address module 30 copies the compressed texture information 22 from the memory 20 into the cache 40. Once the required texture data for the texturing operation is present in the cache 40, the texture address module 30 provides control information, which can include address and control signals, to the cache 40 such that the cache 40 provides the required texture data 42 at its outputs.

See '428 patent at 4:19-46.

B. The '935 Patent

The '935 patent was filed on April 21, 2000 and issued on October 7, 2003, to inventors Ralph Clayton Taylor, Michael Andrew Mang, and Michael Mantor.³ The title of the '935 patent is: "Geometric Engine Including a Computational Module for Use in a Video Graphics Controller." The '935 patent relates generally to a computation module and/or geometric engine for use in a video graphics processing circuit. *See* '935 patent at 1:6-8, 2:26-28. The computation module includes memory, a computation engine, a plurality of thread controllers, and an arbitration module coupled to the plurality of thread controllers. The arbitration module utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine such that idle time of the computation engine is minimized. For example, claim 1 of the '935 patent recites:

A computation module comprises:

³ The effective date of the '428 patent pre-dates the America Invents Act ("AIA") enacted by Congress on September 16, 2011.

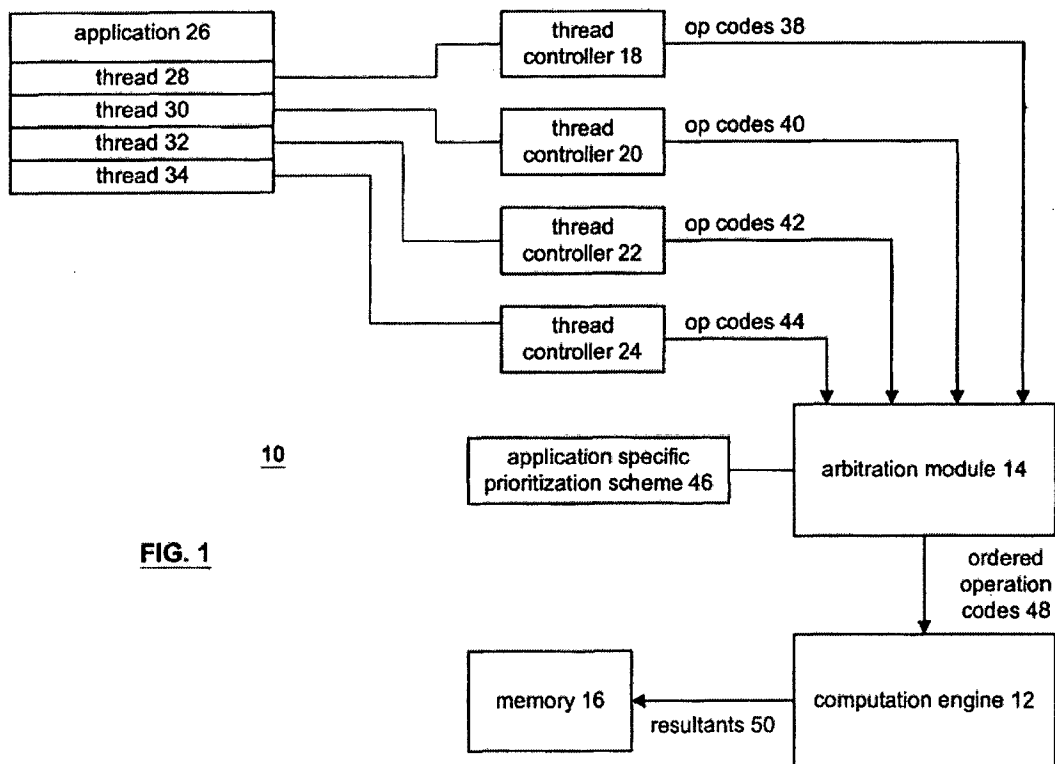
memory;

a computation engine operable to perform an operation based on an operation code and to provide a corresponding result to the memory as indicated by the operation code;

a plurality of thread controllers, wherein each of the plurality of thread controllers manages at least one corresponding thread of a plurality of threads, wherein the plurality of threads constitutes an application, and wherein each of the plurality of threads includes at least one operation code; and

an arbitration module operably coupled to the plurality of thread controllers, wherein the arbitration module utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine in an order to minimize idle time of the computation engine.

Figure 1 of the '935 patent, reproduced below, illustrates a computation module 10 including a computation engine 12, an arbitration module 14, memory 16, and a plurality of thread controllers 18-24.



The arbitration module 14 receives the operation codes 38-44 from the thread controllers 18-24 and, based on an application specific prioritization scheme 46, orders the operation codes to produce ordered operation codes 48 [which] are provided to the computation engine 12.

See '935 patent at 3:48-53. Figure 7 of the '935 patent, reproduced below, illustrates an example of prioritization of operation codes in accordance with the invention.

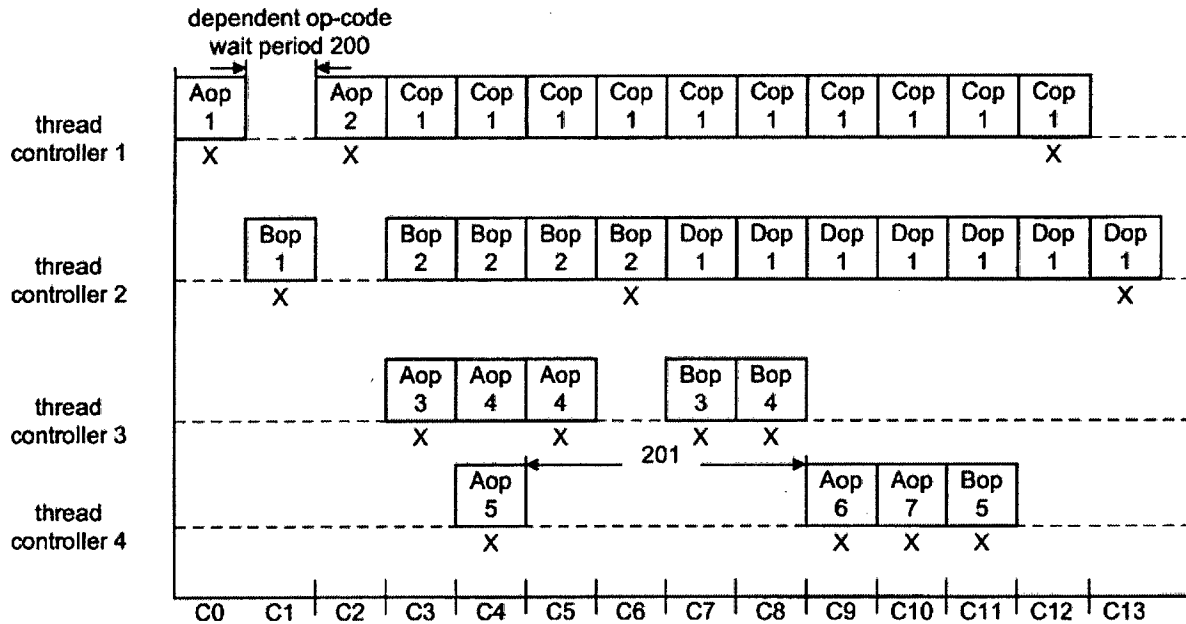


FIG. 7

prioritization scheme

thread 4
thread 3
thread 2; thread 1

X indicates selected by arbitration module based on priority scheme

The specification explains:

FIG. 7 also illustrates a prioritization scheme that indicates a first level of prioritization. As is shown, thread 4 has the highest priority. Based on the discussion presented above, thread 4 may correspond to post-clip processing operations for vertices of a primitive. Thus, the operations performed by thread 4 may result in final result data that is passed downstream to other circuitry and therefore represents the completion of processing for vertices of a primitive. Threads 1 and 2, which may correspond to transform operations on a vertex (initial processing of a vertex), have the lowest priority. Within each level of the priority scheme, additional priority may be given to vertices that have been in the processing pipeline for the greatest length of time. In other words,

if two thread controllers were to share a priority level and both had operation codes pending, the operation code corresponding to the vertex that had been in the pipeline longer would be given priority.

See '935 patent at 31:24-40.

III. LEGAL STANDARDS

Claim construction is a “matter of law exclusively for the court.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. See *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). In construing disputed terms, the Court should first look at the claims themselves, for “[i]t is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Inova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)).

In addition, the claims “must be read in view of the specification, of which they are a part.” *Id.* at 1315 (quoting *Markman*, 52 F.3d at 979). As the Federal Circuit explained in *Phillips*, the specification “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.” *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). The Federal Circuit concluded that “[t]he construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.” *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the specification, courts “should also consider the patent’s prosecution history, if it is in evidence.” *Id.* at 1317 (quoting *Markman*, 52 F.3d at 980). The Federal Circuit

explained that the prosecution history which is “part of the intrinsic evidence, consists of the complete record of the proceedings before the PTO [(U.S. Patent and Trademark Office)] and includes the prior art cited during the examination of the patent.” *Id.* (citation omitted). The Federal Circuit cautioned that “because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes. *Id.* (citation omitted). “Nonetheless, the prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Id.* (citation omitted).

While extrinsic evidence “can shed useful light on the relevant art,” it is “less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Importantly, the extrinsic evidence may not be used to contradict the claim language or the patent specification. *See Vitronics*, 90 F.3d at 1584 (“[E]xtrinsic evidence . . . may be used only to help the court come to the proper understanding of the claims; it may not be used to vary or contradict the claim language. Nor may it contradict the import of other parts of the specification.”) (citations omitted).

The construction of a claim term is generally guided by its ordinary meaning. However, courts may deviate from the ordinary meaning when: (1) “the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention”; or (2) “the patentee acted as his own lexicographer and clearly set forth a definition of the

disputed claim term in either the specification or prosecution history.” *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009). *See also Omega Engineering, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) (“[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.”); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) (“The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution.”). Nevertheless, there is a “heavy presumption that a claim term carries its ordinary and customary meaning.” *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citations omitted). The standard for deviating from the plain and ordinary meaning is “exacting” and requires “a clear and unmistakable disclaimer.” *Thorner v. Sony Computer Entm’t Am. LLC*, 669 F.3d 1362, 1366-67 (Fed. Cir. 2012). *See also Epistar Corp. v. Int’l Trade Comm’n*, 566 F.3d 1321, 1334 (Fed. Cir. 2009) (requiring “expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope” to deviate from the ordinary meaning) (citation omitted).

Courts are not required to construe every claim limitation of an asserted patent. *See O2 Micro Intern. Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (citations omitted). *See also U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (stating that claim construction “is not an obligatory exercise in redundancy.”). Rather, “claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement.” *O2 Micro*, 521 F.3d at 1362 (quoting *U.S. Surgical*, 103 F.3d at 1568). *See also Embrex, Inc. v. Serv. Eng’g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000) (“The

construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims.”) (citation omitted). In addition, “[a] determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.” *O2 Micro*, 521 F.3d at 1361.

Furthermore, a court may construe a claim term as a “means-plus-function” limitation in accordance with 35 U.S.C. § 112, ¶ 6, which provides:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

See 35 U.S.C. § 112, ¶ 6.⁴

While a claim phrase that lacks the term “means” is presumptively not subject to 35 U.S.C. § 112, ¶ 6, that presumption is rebuttable where “the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function.” *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (*en banc*) (citation omitted). In *Williamson*, the Federal Circuit “expressly overrule[d] the characterization of that presumption as ‘strong’ [and] overrule[d] the strict requirement of ‘a showing that the limitation essentially is devoid of anything that can be construed as structure.’” *Id.* at 1349.

The “means-plus-function” analysis is a two-step process. *See also Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1097 (Fed. Cir. 2014). In the first step, courts determine if a claim term invokes § 112, ¶ 6. *Id.* In the second step, if the claim term does invoke § 112, ¶ 6, the

⁴ The pre-AIA version of the cited statute applies to the asserted patents.

disputed claim term is construed by identifying the “corresponding structure, material, or acts described in the specification” to which the claim term will be limited. *Id.* (citing *Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1097 (Fed. Cir. 2008)). If no “corresponding structure, material, or acts described in the specification” can be identified, the claim term is indefinite. *Id.* (citing *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1312 (Fed. Cir. 2012)).

Still further, claim construction may include a determination of claim indefiniteness under 35 U.S.C. § 112, ¶ 2, as a “legal conclusion that is drawn from the court’s performance of its duty as the construer of patent claims.” *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1378 (Fed. Cir. 1999) (quoting *Personalized Media Communications, LLC v. International Trade Comm’n*, 161 F.3d 696, 705 (Fed. Cir. 1998)). Statutory definiteness mandates that the patent specification “conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.” 35 U.S.C. § 112, ¶ 2. “[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014).

IV. THE PERSON OF ORDINARY SKILL IN THE ART

A. Legal Standards

Patent claims are construed from the perspective of a person of ordinary skill in the art:

It is the person of ordinary skill in the field of the invention through whose eyes the claims are construed. Such person is deemed to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field. The inventor’s words that are used to describe the invention--the inventor’s lexicography--must be understood and interpreted by the court as they would be understood and interpreted by a person in that field of technology. Thus, the court starts the decision making process

by reviewing the same resources as would that person, viz., the patent specification and the prosecution history.

Phillips, 415 F.3d at 1313 (quoting *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998)).

“Factors that may be considered in determining level of skill include: type of problems encountered in art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.”

Mintz v. Dietz & Watson, Inc., 679 F.3d 1372, 1376 (Fed. Cir. 2012) (quoting *Custom Accessories, Inc. v. Jeffrey-Allan Industries, Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

B. The Computer Graphics Patents ('428, '935, and '945 Patents)

Complainant AST argues that “[a] person of ordinary skill in the art would have a degree in electrical engineering, computer engineering, computer science, or a related field, and at least 3-5 years’ experience working in computer graphics hardware, computer architecture, or related fields, or an equivalent combination of graduate education and/or work experience.” (See CIMB at 12, 45, 76.)

Respondents disagree with respect to the level of professional experience (2-3 years instead of 3-5 years) and propose that “a person of ordinary skill in the art would have a B.S. degree in electrical engineering, computer science, or an equivalent field as well as at least 2-3 years of academic or industry experience in computer graphics, image processing hardware, general computer architecture, or comparable industry experience.” (See RIMB at 1.)

The Staff’s proposed level of skill in the art is consistent with that proposed by Respondents, namely: “a Bachelor’s degree in electrical engineering, computer engineering, computer science, or an equivalent field, along with at least two years of relevant academic or

industry experience in video graphics technology, image processing, computer architecture, or comparable industry experience.” (See SMB at 9, 24-25, 50.)

As noted during the *Markman* hearing, “[t]he [asserted] patents relate to a rather complex technology, and three years of professional experience seem more appropriate than two years.” (See June 20, 2016 *Markman* Tr. at 14:10-12.) Accordingly, I find that a person of ordinary skill in the art would have a Bachelor’s degree in electrical engineering, computer engineering, computer science, or an equivalent field as well as at least three (3) years of academic or industry experience in computer graphics, image processing hardware, computer architecture, or comparable industry experience.

C. The Memory Systems Patent (’439 Patent)

Complainant AST argues that “[a] person of ordinary skill in the art would have a degree in electrical or computer engineering, or a related field, and at least 3-5 years' experience working in memory systems hardware, computer architecture, or related fields, or an equivalent combination of graduate education and/or work experience.” (See CIMB at 34.)

Respondents again disagree with respect to the level of professional experience (2 years instead of 3-5 years) argue that “a person of ordinary skill in the art would have a Bachelor’s degree in electrical engineering or computer engineering, or at least a Bachelor’s degree in computer science with a minimum of two years of academic or work experience in computer systems.” (See RIMB at 1-2.)

The Staff’s proposed level of skill in the art is consistent with that proposed by Respondents, namely: “a Bachelor’s degree in electrical engineering, computer engineering, computer science, or an equivalent field, along with at least two years of relevant academic or

industry experience in memory systems technology, computer architecture, or comparable industry experience.” (See SMB at 19-20.)

As noted during the *Markman* hearing, “[t]he [asserted] patents relate to a rather complex technology, and three years of professional experience seem more appropriate than two years.” (See June 20, 2016 *Markman* Tr. at 14:10-12.) Accordingly, I find that a person of ordinary skill in the art would have a Bachelor’s degree in electrical engineering, computer engineering, computer science, or an equivalent field as well as at least three (3) years of academic or industry experience in memory systems technology, computer architecture, or comparable industry experience.

V. CLAIM CONSTRUCTION OF DISPUTED TERMS

A. ’428 Patent Disputed Term: “texture address module”

The parties’ respective constructions for the disputed term “texture address module” appear in the table below.

Term	AST	Respondents	Staff
“texture address module” (’428 patent, claims 1 and 10)	Plain and ordinary meaning.	Subject to 35 U.S.C. § 112, ¶ 6. <u>Structure</u> : none; indefinite	Should be construed according to 35 U.S.C. § 112, ¶ 6. <u>Structure</u> : The subset of the video graphics texture mapping circuit that contains texture address circuitry and electrical connections to the cache/s and [memory].

In construing disputed terms, courts should first look at the language of the claims. See *Phillips*, 415 F.3d at 1312.

Claim 1 of the ’428 patent recites:

A video graphics texture mapping circuit, comprising:

memory storing compressed texture information corresponding to at least one texture;

a cache operably coupled to the memory, wherein the cache stores a portion of the compressed texture information;

a texture address module operably coupled to the memory and the cache, wherein the texture address module determines whether texture data for a texturing operation is stored in the cache, wherein when the texture data is not stored in the cache, the texture address module copies the texture data from the memory to the cache, wherein the texture address module provides control information to the cache such that the cache outputs the texture data; and

a decompression block operably coupled to the cache, wherein the decompression block decompresses the texture data to produce uncompressed texture data for use in the texturing operation.

Claim 10 recites:

A video graphics texture mapping circuit comprising:

memory storing compressed texture information corresponding to at least one texture;

a plurality of caches operably coupled to the memory, wherein each of the plurality of caches stores a portion of the compressed texture information;

a texture address module operably coupled to the memory and the plurality of caches, wherein the texture address module determines whether texture data for at least one texturing operation is stored in the plurality of caches such that the texture data is available for the at least one texturing operation, wherein when the texture data is not stored in the plurality of caches such that the texture data is available for the at least one texturing operation, the texture address module copies needed portions of the texture data from the memory to at least one of the plurality of caches, wherein the texture address module provides control information to the plurality of caches such that the texture data for the texturing operations is provided at outputs of the plurality of caches; and

a plurality of decompression blocks operably coupled to the plurality of caches, wherein the plurality of decompression blocks decompress the texture data provided at the outputs of the plurality

of caches to produce uncompressed texture data for the at least one texturing operation.

1. Parties' Arguments

Complainant AST argues that “texture address module” has a plain and ordinary meaning that connotes structure to those of ordinary skill in the art (*e.g.*, texture circuitry), and should not be construed according to 35 U.S.C. § 112, ¶ 6. (*See* CIMB at 25 (providing technical dictionary meaning of “texture” and “address”).) In addition, Complainant argues that the claim language requiring the “texture address module” to be operably coupled to circuit elements, including the cache and the memory, shows that “it too must be a circuit element.” (*See id.* at 19.)

Respondents argue that “texture address module” does not have a well-understood structural meaning in the video graphics field and is not defined in the specification. (*See* RIMB at 11.) In addition, Respondents argue that “texture address” does not impart structural significance to the term “module.” (*See id.* at 12.) Respondents conclude that “texture address module” should be construed under 35 U.S.C. § 112, ¶ 6. Further, while Respondents admit that the specification describes the “texture address module” as being part of the “video graphics texture mapping circuit,” they argue that “[t]he texture address module term is indefinite because the specification fails to set forth corresponding structure to perform the recited functions.” (*See id.* at 14.)

The Staff argues that “texture address module” does not have a plain and ordinary meaning and should be construed according to 35 U.S.C. § 112, ¶ 6. (*See* SMB at 14.) The Staff further argues that “texture address module” is not indefinite and that the ’428 patent specification sufficiently discloses a definitive structure corresponding to the “texture address module,” namely “[t]he subset of the video graphics texture mapping circuit that contains texture address circuitry and electrical connections to the cache/s and memory.” (*See id.* at 12, 16.)

2. Applicability of § 112, ¶ 6

I find that the claim language as a whole, *i.e.*, “texture address module operably coupled to the memory and the cache [or the plurality of caches],” connotes sufficiently definite structure or acts such that § 112, ¶ 6 does not apply.

The claim language “texture address module operably coupled to the memory and the cache [or the plurality of caches]” does not include the word “means.” Therefore, there is a presumption that the disputed claim language does not invoke § 112, ¶ 6. However, “[m]erely because an element does not include the word ‘means’ does not automatically prevent that element from being construed as a means-plus function element.” *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 531 (Fed. Cir. 1996).

As noted in *Williamson*, “module” is a “nonce word that can operate as a substitute for ‘means’.” *Williamson*, 792 F.3d at 1350. But the rest of the disputed claim language recites sufficiently definite structure or acts to perform the claimed function such that § 112, ¶ 6 does not apply. *See Mass. Inst. of Tech. & Elecs. for Imaging, Inc. v. Abacus Software*, 462 F.3d 1344, 1354 (Fed. Cir. 2006) (recognizing that surrounding claim language can add sufficient structure to avoid a § 112, ¶ 6 construction). The term “module” is modified by “texture address” and the limitation “texture address module” is claimed as being “operably coupled to the memory and the cache or plurality of caches.” This claim language imparts structural significance to the term “module” and shows that the “texture address module” is a specific type of circuit element. Thus, the claim language demonstrates the term “texture address module” refers to a discrete structure well-known to those of ordinary skill in the art for performing the claimed functions. (*See* CIMB at 23.) *See also* SMB at 17 (“One of ordinary skill in the art would [] understand that the operable coupling limitation imparts definitive structure of circuitry to the ‘texture address module’ because it cannot be ‘operably coupled’ to circuit elements such

as the cache and the memory unless the ‘texture address module’ is, in and of itself, a circuit.”). The claim language also specifies how the “texture address module” is to be implemented in the invention, further solidifying its definiteness. (*See e.g.*, ‘428 patent, claim 1 (“the texture address module determines whether texture data for a texturing operation is stored in the cache,” “when the texture data is not stored in the cache, the texture address module copies the texture data from the memory to the cache,” and “the texture address module provides control information to the cache such that the cache outputs the texture data.”).)

The specification confirms this conclusion by consistently referring to the “texture address module” as a circuit element. *See, e.g.*, CIMB at 19; ‘428 patent at 3:34-36 (“The video graphics texture mapping circuit 10 includes a memory 20, a cache 40, a texture address module 30, and a decompression block 50.”), Figures 1-2. Thus, I find, based on the intrinsic record, that “texture address module” connotes sufficiently definite structure to a person of ordinary skill in the art. Accordingly, I find the presumption against construing the term as means-plus-function under § 112, ¶ 6 has not been rebutted. *See also* SMB at 12, 16-17 (Staff’s proposed structure corresponding to the “texture address module” refers to a discrete class of structures, i.e., “[t]he subset of the video graphics texture mapping circuit that contains texture address circuitry and electrical connections to the cache/s and memory”). *Compare Williamson*, 792 F.3d at 1351 (“At bottom, we find nothing in the specification or prosecution history that might lead us to construe that expression as the name of a sufficiently definite structure as to take the overall claim limitation out of the ambit of § 112, para. 6.”); *Certain Table Saws Incorporating Active Injury Mitigation Technology & Components Thereof*, Inv. No. 337-TA-965, Order No. 11 at 21-22 (U.S.I.T.C. Apr. 29, 2016) (Pender, J) (finding “‘detection’ to impart structural significance to

the term ‘system’ by referencing a discrete class of structures (*i.e.*, detectors) well known to those of ordinary skill in the art for performing the claimed functions”).

3. Construction Analysis

I find the phrase “texture address module” has a plain and ordinary meaning to those of ordinary skill in the art. Complainant agrees. (*See* CIMB at 25 (stating that “texture” in computer graphics means “shading or other attributes added to the ‘surface’ of a graphical image to give it the illusion of a physical substance” and “address” means “a number specifying a location in memory where data is stored”) (citing Microsoft Dictionary of Computer Terms, p. 17, p. 465 (3rd ed., Microsoft Press 1997)); Hart Decl. at ¶¶ 29, 38.) Likewise, so do Respondents. (*See* June 20 *Markman* Tr. at 72:19-21 (“Texture address has a plain and ordinary meaning. It is the address of a texture in memory.”).)

There is no indication in the specification the patent applicant acted as his or her own lexicographer or the applicant disclaimed any part of the phrase’s plain and ordinary meaning. To the contrary, the intrinsic record (*i.e.*, both the claim language and specification) uses the term “texture address module” consistent with its understood plain and ordinary meaning. (*See e.g.*, ’428 patent at 4:35-45 (“As such, a texture address module 30 is used to determine whether or not the texture data for a particular texturing operation is currently stored in the cache 40. When the texture data is not stored in the cache 40, the texture address module 30 copies the compressed texture information 22 from the memory 20 into the cache 40. Once the required texture data for the texturing operation is present in the cache 40, the texture address module 30 provides control information, which can include address and control signals, to the cache 40 such that the cache 40 provides the required texture data 42 at its outputs.”), 5:66-6:2 (“The video graphics texture mapping circuit 100 of FIG. 2 includes the memory 20, the texture address

module 30, a plurality of caches 40 and 120, and a plurality of decompression blocks 50 and 160.”.)

Respondents and the Staff argue claim 1 recites “additional functions” for the “texture address module.” *See, e.g.*, June 20, 2016 *Markman* Tr. at 111:6-13. While I agree those additional claim limitations serve to further limit the scope of the term, it would be redundant, and thus improper, to include them in the construction of the term “texture address module.” Moreover, they do not rebut the heavy presumption that a claim term carries its ordinary and customary meaning. *See CCS Fitness*, 288 F.3d at 1366.

Courts are not required to construe every claim limitation of an asserted patent. *See U.S. Surgical*, 103 F.3d at 1568 (stating that claim construction “is not an obligatory exercise in redundancy.”). Rather, “claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement.” *See O2 Micro*, 521 F.3d at 1362. *Compare id.* at 1361 (“A determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.”). Here, there appears to be no dispute between the parties that the phrase has a commonly understood meaning to one of skill in the art.

Accordingly, I find that “texture address module” should be construed in accordance with its plain and ordinary meaning. In addition, I find that “texture address module” is readily understood by persons of ordinary skill in the art and requires no further construction.

B. '935 Patent Disputed Terms

1. "arbitration module"

The parties' respective constructions for the disputed term "arbitration module" appear in the table below.

Term	AST	Respondents	Staff
"arbitration module" ('935 patent, claim 1)	Plain and ordinary meaning.	Subject to 35 U.S.C. § 112, ¶ 6. <u>Structure</u> : Indefinite	Should be construed according to 35 U.S.C. § 112 ¶ 6. <u>Structure</u> : An arbiter element that is coupled to the [thread controllers] and the [computation engine].

In construing disputed terms, the Court should first look at the claims themselves, for "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *See Phillips*, 415 F.3d at 1312 (citations omitted).

Claim 1 recites:

A computation module comprises:

memory;

a computation engine operable to perform an operation based on an operation code and to provide a corresponding result to the memory as indicated by the operation code;

a plurality of thread controllers, wherein each of the plurality of thread controllers manages at least one corresponding thread of a plurality of threads, wherein the plurality of threads constitutes an application, and wherein each of the plurality of threads includes at least one operation code; and

an **arbitration module** operably coupled to the plurality of thread controllers, wherein the **arbitration module** utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation

engine in an order to minimize idle time of the computation engine.

a. Parties' Arguments

Complainant AST argues that “arbitration module” has a plain and ordinary meaning that connotes structure to those of ordinary skill in the art (*e.g.*, circuitry), and should not be construed according to 35 U.S.C. § 112, ¶ 6. (*See* CIMB at 54-56 (providing technical dictionary meaning of “arbitration” and “arbiter” which are used interchangeably in the ’935 patent) (citing ’935 patent at 19:31-36, 19:51-53; Dictionary of Scientific and Technical Terms (5th ed. McGraw Hill 1994) (defining “arbiter” as “[a] computer unit that determines the priority sequence in which two or more processor inputs are connected to a single functional unit such as a multiplier or memory.”). In addition, Complainant argues that the claim language requiring the “arbitration module” to be operably coupled to the plurality of thread controllers, shows that “the arbitration module must also be a circuit.” (*See id.* at 54.)

Respondents argue that “arbitration module” does not connote a specific structure to one of ordinary skill in the art. (*See* RIMB at 34.) Respondents conclude that “arbitration module” should be construed under 35 U.S.C. § 112, ¶ 6. Further, Respondents argue that “arbitration module” is indefinite because the specification “does not allow one of ordinary skill in the art to recognize which specific structure or structures achieve the stated function of the arbitration module.” (*See id.* at 38.)

The Staff argues that “arbitration module” does not have a plain and ordinary meaning and should be construed according to 35 U.S.C. § 112, ¶ 6. (*See* SMB at 38.) But the Staff agrees with AST that “arbitration module” and “arbiter” are used interchangeably in the ’935 patent specification. (*See* SMB at 39 (“The specification uses the term ‘arbitration module’ interchangeably with the term ‘arbiter,’ which, to those of ordinary skill in the art, connotes

particular circuitry structure.”.) The Staff concludes that “arbitration module” is not indefinite and that the ’935 patent specification sufficiently discloses a definitive structure corresponding to the “arbitration module.” (*See id.* at 39-41.)

b. Applicability of § 112, ¶ 6

I find that the claim language as a whole, *i.e.*, “arbitration module operably coupled to the plurality of thread controllers,” connotes sufficiently definite structure or acts such that § 112, ¶ 6 does not apply.

The claim language “arbitration module operably coupled to the plurality of thread controllers” does not include the word “means.” Therefore, there is a presumption that the disputed claim language does not invoke § 112, ¶ 6. However, “[m]erely because an element does not include the word ‘means’ does not automatically prevent that element from being construed as a means-plus function element.” *Cole v. Kimberly-Clark Corp.*, 102 F.3d 524, 531 (Fed. Cir. 1996).

As noted in *Williamson*, “module” is a “nonce word that can operate as a substitute for ‘means’.” *Williamson*, 792 F.3d at 1350. But the rest of the disputed claim language recites sufficiently definite structure or acts to perform the claimed function such that § 112(f) does not apply. *See Mass. Inst. of Tech.*, 462 F.3d at 1354 (recognizing that surrounding claim language can add sufficient structure to avoid a § 112 ¶ 6 construction). The term “module” is modified by “arbitration” and the limitation “arbitration module” is claimed as being “operably coupled to the plurality of thread controllers.” This claim language imparts structural significance to the term “module” and shows that the “arbitration module” is a specific type of circuit element. Thus, the claim language shows that the term “arbitration module” refers to a discrete structure well-known to those of ordinary skill in the art for performing the claimed functions. (*See CIMB* at 54; *SMB* at 39.)

The specification confirms this conclusion by consistently referring to the “arbitration module” as a circuit element. *See, e.g.*, CIMB at 55 (“Figure 11 of the ’935 Patent . . . discloses ‘a block diagram of a circuit that provides shared microcode to a plurality of thread controllers in accordance with a particular embodiment of the present invention.’”) (citing ’935 patent at 2:18-21); SMB at 40 (citing ’935 patent at 2:18-21, 15:24-52, Figure 11). The specification also uses “arbitration module” and “arbiter” interchangeably (*accord* SMB at 39). *See, e.g.*, ’935 patent at 19:31-36, 19:51-53:

Because the actual operation codes to be executed can be determined through the use of microcode generation block 620, the amount of information that must be provided by each of the thread controllers 601-603 to the **arbitration module 610** which is then passed on to the microcode generation block 620 is reduced.

...

By moving the microcode “behind” the **arbiter** with respect to the viewpoint of the thread controllers, the thread controllers are greatly simplified.

See also Figure 11, reproduced below:

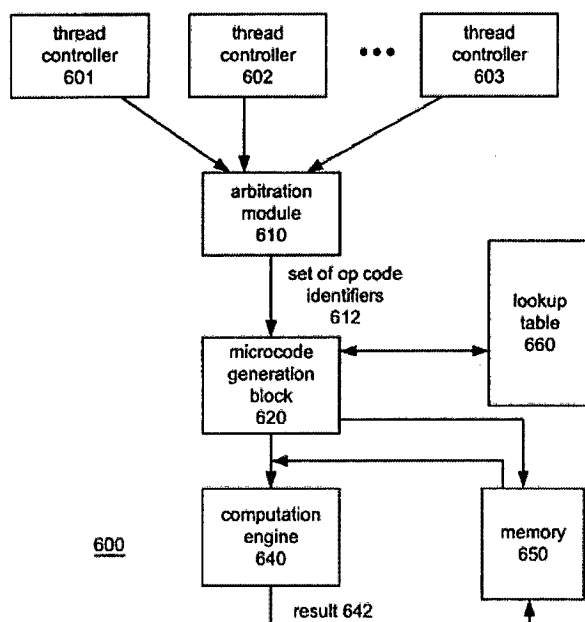


FIG. 11

See also Figure 7, reproduced *supra* section II(B) (stating that “X indicates selected by arbitration module based on priority scheme”); *compare* ’935 patent at 32:6-8 (“[T]he arbiter can select from operation codes Cop1, Bop2, and Aop3 during cycle C3.”).

Thus, I find based on the intrinsic record “arbitration module” connotes sufficiently definite structure to one of ordinary skill in the art. Accordingly, I find the presumption against construing the term as means-plus-function under § 112, ¶ 6 has not been rebutted. See also SMB at 37 (Staff’s proposed structure corresponding to the “arbitration module” refers to a discrete class of structures, *i.e.*, “[a]n arbiter element that is coupled to the [thread controllers] and the [computation engine].”). Compare *Williamson*, 792 F.3d at 1351 (“At bottom, we find nothing in the specification or prosecution history that might lead us to construe that expression as the name of a sufficiently definite structure as to take the overall claim limitation out of the ambit of § 112, para. 6.”); *Certain Table Saws Incorporating Active Injury Mitigation Technology & Components Thereof*, Inv. No. 337-TA-965, Order No. 11 at 21-22 (U.S.I.T.C. Apr. 29, 2016) (Pender, J) (finding “‘detection’ to impart structural significance to the term ‘system’ by referencing a discrete class of structures (*i.e.*, detectors) well known to those of ordinary skill in the art for performing the claimed functions”).

c. Construction Analysis

I find the phrase “arbitration module” has a plain and ordinary meaning. As noted by Complainant AST, the terms “arbitration” or “arbiter” have a well-known meaning in this art. (See CIMB at 56; Hart Decl. at ¶ 60.) Respondents and the Staff do not dispute AST’s technical definitions. See, *e.g.*, June 20, 2016 *Markman* Tr. at 155:20-24 (“[Arbiter] is known as a structure. And I don’t dispute that.”).

There is no indication in the specification the patent applicant acted as his or her own lexicographer or the applicant disclaimed any part of the phrase’s plain and ordinary meaning.

To the contrary, the intrinsic record (*i.e.*, both the claim language and specification) uses the term “arbitration module” consistent with its understood plain and ordinary meaning. (*See e.g.*, ’935 patent at 2:52-59 (“The arbitration module is coupled to the plurality of thread controllers and utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine such that idle time of the computation engine is minimized. The prioritization scheme prioritizes certain threads over other threads such that the throughput through the computation module is maximized.”), 4:9-15 (“The objective of the arbitration module 14 is to order the operation codes 48 such that the computation engine 12 runs at capacity (*i.e.* the pipeline within the computation engine is always full and the resources in the computation engine are efficiently utilized). Thus, for every operation cycle of the computation engine 12, the arbitration module 14 attempts to provide it with an operation code for execution.”), 16:35-45 (“The arbitration module 610 determines an order of execution of command codes corresponding to the sets of operation code identifiers that it receives from the plurality of thread controllers 601-603. The arbitration module preferably performs this determination based on some type of prioritization scheme that is described in additional detail with respect to FIG. 6 below. Once the arbitration module 610 has selected a particular set of operation code identifiers to be executed during the next cycle, the arbitration module 610 passes that selected set of operation code (op code) identifiers 612 to the microcode generation block 620.”))

Respondents and the Staff argue claim 1 recites “additional functions” for the “arbitration module.” *See, e.g.*, June 20, 2016 *Markman* Tr. at 162:10-13. While I agree those additional claim limitations serve to further limit the scope of the term, it would be redundant, and thus improper, to include them in the construction of the term “arbitration module.” Moreover, they

do not rebut the heavy presumption that a claim term carries its ordinary and customary meaning. *See CCS Fitness*, 288 F.3d at 1366.

Courts are not required to construe every claim limitation of an asserted patent. *See U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (stating that claim construction “is not an obligatory exercise in redundancy.”). Rather, “claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement.” *See O2 Micro*, 521 F.3d at 1362. *Compare id.* at 1361 (“A determination that a claim term ‘needs no construction’ or has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.”). Here, there appears to be no dispute between the parties that the phrase has a commonly understood meaning to one of skill in the art.

Accordingly, I find that “arbitration module” should be construed in accordance with its plain and ordinary meaning. In addition, I find that “arbitration module” is readily understood by persons of ordinary skill in the art and requires no further construction.

2. “operation code”

The parties’ respective constructions for the disputed term “operation code” appear in the table below.

Term	AST	Respondents	Staff
“operation code” (’935 patent, claims 1 and 7)	Plain and ordinary meaning.	A computer instruction that includes a thread identifier that identifies the particular [thread controller] that issued the instruction, a type of operation to be performed, a first source address, a second source address, and a destination address.	Plain and ordinary meaning, for example: a computer instruction, which may include a thread identifier that identifies the particular [thread controller] that issued the instruction, a type of operation to be performed, a first source address, a second source address, and a destination address.

In construing disputed terms, the Court should first look at the claims themselves, for “[i]t is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *See Phillips*, 415 F.3d at 1312.

Claim 1 recites:

A computation module comprises:

memory;

a computation engine operable to perform an operation based on an **operation code** and to provide a corresponding result to the memory as indicated by the **operation code**;

a plurality of thread controllers, wherein each of the plurality of thread controllers manages at least one corresponding thread of a plurality of threads, wherein the plurality of threads constitutes an application, and wherein each of the plurality of threads includes at least one **operation code**; and

an arbitration module operably coupled to the plurality of thread controllers, wherein the arbitration module utilizes an application specific prioritization scheme to provide **operation codes** from the plurality of thread controllers to the computation engine in an order to minimize idle time of the computation engine.

Claim 7 recites:

The computation engine of claim 1, wherein each thread of the plurality of threads includes a sequence of **operation codes** corresponding to a predetermined portion of the application.

a. Parties’ Arguments

Complainant AST and the Staff argue that “operation code” should be given its plain and ordinary meaning. Respondents argue that the patentee “deviated from the ordinary meaning of ‘operation code’ by defining the term in their invention to include more than just the operation to be performed.” (*See* RIMB at 29-30.) Specifically, Respondents argue that “operation code” should be construed as “a computer instruction that includes a thread identifier that identifies the

particular [thread controller] that issued the instruction, a type of operation to be performed, a first source address, a second source address, and a destination address.” Respondents reason that “the operation code must have thread identifier information, so that the arbitration module can prioritize an operation code of one thread ahead of an operation code from another thread.” (See RIMB at 30.)

b. Construction Analysis

There is a “heavy presumption that a claim term carries its ordinary and customary meaning.” See *CCS Fitness*, 288 F.3d at 1366. The standard for deviating from the plain and ordinary meaning is “exacting” and requires “a clear and unmistakable disclaimer.” See *Thorner*, 669 F.3d at 1366-67. See also *Epistar*, 566 F.3d at 1334 (requiring “expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope” to deviate from the ordinary meaning).

As noted by Complainant AST, the term “operation code” is a term of art that has a well-established meaning. (See CIMB at 50-51 (citing, e.g., The IEEE Standard Dictionary of Electrical and Electronics Terms, p. 717 (6th ed., IEEE 1999) (defining “opcode” as “[a] bit pattern that identifies a particular instruction.”)); Hart Decl. at ¶¶ 51-55, 57, 58.) Respondents do not dispute what the plain and ordinary meaning of operation code is, but argue that the patentee deviated from such meaning. See June 20 *Markman* Tr. at 191:15-18 (“So we have an agreement on what the ordinary meaning of op code is. The question in this case, your Honor, is whether the patentees did something different with that ordinary meaning.”).

Respondents cite portions of the specification describing exemplary embodiments. See ’935 patent at 3:19-23 (relating to a discussion of Figure 1), 3:11-33 (same); 4:16-28 (same), 12:15-25 (relating to a discussion of Figure 10), 15:52-56 (relating to a discussion of Figure 11). But see *id.* at 2:61-63 (“FIG. 1 illustrates a computation module 10 that may bemused[sic] in a

geometric engine of a video graphics circuit.”); 11:31-32 (FIG. 10 illustrates a circuit 500 that may be included in the vector engine 92 as illustrated in FIG. 3.”), 15:24-28 (“FIG. 11 illustrates a multi-thread processing circuit 600 that includes a plurality of thread controllers 601-603, where each of the thread controllers 601-603 manages processing operations for a particular operation. In one example embodiment . . .”). *See also id.* at 8:52-55 (“the particular operation code being executed may include the addressing information (source address) require[d] to access the memory 350.”), 10:66-11:5 (“The operation code provided by each thread preferably includes thread identity information.”). Thus, the embodiments are prefaced with permissive, non-compulsory language. *See SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (“Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim, limitations that are not a part of the claim.”).

In addition, as noted by the Staff, claim 3 already requires the operation code to include “a controller identity, a type of operation, a first source address, a second source address, and a destination address.” (*See* SMB at 32-33.) Thus, the doctrine of claim differentiation creates a presumption that the “operation code” of independent claim 1 is broader than dependent claim 3. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004) (“As this court has frequently stated, the presence of a dependent claim that adds a particular limitation raises a presumption that the limitation in question is not found in the independent claim.”); *see also id.* (“[W]here the limitation that is sought to be ‘read into’ an independent claim already appears in a dependent claim, the doctrine of claim differentiation is at its strongest.”).

Accordingly, I find no clear and unmistakable disavowal of claim scope and construe “operation code” in accordance with its plain and ordinary meaning. There is no dispute

between the parties as to that plain and ordinary meaning. Thus, I find that “operation code” requires no construction. *See O2 Micro*, 521 F.3d at 1362 (“[C]laim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement.”).

3. “computation engine”

The parties’ respective constructions for the disputed term “computation engine” appear in the table below.

Term	AST	Respondents	Staff
“computation engine” (’935 patent, claim 1)	Specialized graphics circuitry that receives and executes operation codes and generates results therefrom.	Engine that performs computations.	Plain and ordinary meaning, for example: computing circuitry

In construing disputed terms, the Court should first look at the claims themselves, for “[i]t is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *See Phillips*, 415 F.3d at 1312.

Claim 1 recites:

A computation module comprises:

memory;

a **computation engine** operable to perform an operation based on an operation code and to provide a corresponding result to the memory as indicated by the operation code;

a plurality of thread controllers, wherein each of the plurality of thread controllers manages at least one corresponding thread of a plurality of threads, wherein the plurality of threads constitutes an application, and wherein each of the plurality of threads includes at least one operation code; and

an arbitration module operably coupled to the plurality of thread controllers, wherein the arbitration module utilizes an

application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine in an order to minimize idle time of the computation engine.

a. Parties' Arguments

Complainant AST argues that “computation engine” should be “limited to specialized graphics circuitry” because “the inventors of the ’935 Patent clearly distinguish the claimed ‘computation engine’ over prior art general purpose CPUs that execute software.” (See CIMB at 66-67.)

Respondents and the Staff argue that the term “computation engine” should be construed in accordance with its plain and ordinary meaning. Respondents and the Staff reason that “[n]othing in the specification limits the term to ‘specialized graphics circuitry’ as urged by Complainant.” (See RIMB at 50; *accord* SMB at 26-27.) Rather, Respondents and the Staff argue, “even the larger ‘computation module’ need not be used for processing graphics.” (See RIMB at 50 (citing ’935 patent at 5:65-67 (“FIG. 3 illustrates a block diagram of another computation module 90 that *may* be used in a geometric engine of a video graphics circuit.”) (emphasis added)); *accord* SMB at 27.)

b. Construction Analysis

There is a “heavy presumption that a claim term carries its ordinary and customary meaning.” See *CCS Fitness*, 288 F.3d at 1366. The standard for deviating from the plain and ordinary meaning is “exacting” and requires “a clear and unmistakable disclaimer.” See *Thorner*, 669 F.3d at 1366-67. See also *Epistar*, 566 F.3d at 1334 (requiring “expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope” to deviate from the ordinary meaning).

Complainant AST cites portions of the specification describing exemplary embodiments. *See, e.g.*, CIMB at 65 (citing '935 patent at 6:4-6 (“The vector engine 92 and the scalar engine 94 **may** constitute the computation engine 12 of FIGS. 1 and 2.”) (emphasis added)). *See also* '935 patent at 2:61-63 (“FIG. 1 illustrates a computation module 10 that may bemused[sic] in a geometric engine of a video graphics circuit.”), 5:65-67 (“FIG. 3 illustrates a block diagram of another computation module 90 that may be used in a geometric engine of a video graphics circuit.”). Thus, the '935 patent embodiments are prefaced with permissive, non-compulsory language. *See SuperGuide*, 358 F.3d at 875 (“Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim, limitations that are not a part of the claim.”).

In addition, as noted by Respondents, “dependent claim [8]” recites the term “graphics” but claim 1 does not. *See* June 20, 2016 *Markman* Tr. at 221:7-11; *accord* RRMB at 47-48. *See Liebel-Flarsheim*, 358 F.3d at 910 (“As this court has frequently stated, the presence of a dependent claim that adds a particular limitation raises a presumption that the limitation in question is not found in the independent claim.”).

Thus, I find no clear and unmistakable disavowal of claim scope and construe “computation engine” in accordance with its plain and ordinary meaning. Respondents’ proposed construction does not add any clarification to the claim term. *See O2 Micro Intern. Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) (citations omitted) (“[C]laim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement.”).

Accordingly, I find that “computation engine” should be construed in accordance with its plain and ordinary meaning. In addition, I find that “computation engine” is readily understood by persons of ordinary skill in the art and requires no further construction.

4. “in an order to minimize idle time of the computation engine”

The parties’ respective constructions for the disputed term “computation engine” appear in the table below.

Term	AST	Respondents	Staff
“in an order to minimize the idle time of the computation engine” (’935 patent, claim 1)	In a sequence that increases the number of operations per unit time processed by computation engine relative to an unprioritized scheme	Indefinite	Indefinite, otherwise: In a sequence that minimizes idle time of the [computation engine] and thereby maximizes the throughput of threads through the computation module.

In construing disputed terms, the Court should first look at the claims themselves, for “[i]t is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *See Phillips*, 415 F.3d at 1312 (citations omitted).

Claim 1 recites:

A computation module comprises:

memory;

a computation engine operable to perform an operation based on an operation code and to provide a corresponding result to the memory as indicated by the operation code;

a plurality of thread controllers, wherein each of the plurality of thread controllers manages at least one corresponding thread of a plurality of threads, wherein the plurality of threads constitutes an application, and wherein each of the plurality of threads includes at least one operation code; and

an arbitration module operably coupled to the plurality of thread controllers, wherein the arbitration module utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine **in an order to minimize idle time of the computation engine.**

a. Parties' Arguments

Complainant argues that “in an order to minimize the idle time of the computation engine” should be construed as “in a sequence that increases the number of operations per unit time processed by computation engine relative to an unprioritized scheme.” Complainant reasons that the '935 patent equates minimizing idle time with a higher throughput of the computation engine. (*See* CIMB at 71.)

Respondents and the Staff argue that “minimize” is distinct from “reduce.” Rather, they argue, “minimize” means “reduce to the smallest possible amount,” and as such, the specification and prosecution history provide no guidance or objective boundaries for determining whether idle time has been minimized. (*See* SMB at 47.) Respondents and the Staff further argue that the patentee distinguished “reduce” when it argued during prosecution that the Mallick prior art “reduce[d] access latency.”

Complainants reply that access latency (fetch time) is distinct from idle time of the computation engine. (*See* CRMB at 44.)

b. Construction Analysis

A fundamental dispute between the parties is whether the idle time of the computation engine should be compared to an unprioritized scheme (*i.e.*, a scheme that “would basically submit items to the computational engine in a serial fashion,” *see* June 21, 2016 *Markman* Tr. at 351:15-352:12) or to any and every other prioritized or unprioritized scheme.

While I agree that the ordinary meaning of “minimize” is “reduce to the smallest possible amount,” I disagree with Respondents and the Staff’s narrow view that it must be compared to

any and every other possible prioritization scheme or unprioritized scheme. Not only that is not what is described in the specification, it is not even possible to achieve according to Respondents' own expert. *See, e.g.,* SMB at 48; *accord* RIMB at 62:

A fundamental problem with the inventors' use of the word "minimize" in this context is that a skilled artisan would understand that it is not technically feasible to order a given set of operation codes in such a way as to truly "minimize idle time" of a computation engine. (*See* RMIB, Ex. B, Lastra Decl. at ¶ 30). This is because, in order to truly "minimize" idle time, one would have to execute every single combination and permutation of operation code orderings and compare the respective idle times resulting from each such combination / permutation to determine which reflected the true minimum.

On the other hand, the embodiments in the specification are simply described as reducing idle time of the computation engine with an application specific prioritization scheme. For example, the specification describes the back-to-front prioritization scheme as an example of prioritization scheme (see Fig. 7). *See also* '935 patent at 3:62-66 ("Since the processing of geometric primitives is very structured, the application specific prioritization scheme 46 may prioritize operations in a back-to-front manner that ensures that processing that is nearing completion is prioritized over processing that is just beginning."). But the back-to-front prioritization scheme is not compared to another prioritization scheme. Rather, the logical implication is that the embodiments which utilize an application specific prioritization scheme are compared to the absence of such an application specific prioritization scheme. *See, e.g.,* '935 patent at Abstract:

The arbitration module is coupled to the plurality of thread controllers and utilizes an application specific prioritization scheme to provide operation codes from the plurality of thread controllers to the computation engine such that idle time of the computation engine is minimized. The prioritization scheme prioritizes certain threads over other threads such that the throughput through the computation module is maximized.

See also id. at 28:10-21:

In a prioritization scheme, the operation codes of the barycentric thread 132 may be given priority over other operation codes from the other threads. This helps to force vertices out of the pipeline of the computation engine 110 such that new vertices may be fed into the pipeline for processing. With such a prioritization scheme, vertices are effectively "pulled" through the pipeline from the back end (output end). As a vertex is pulled out (final processing for a vertex is completed), room is made in the pipeline for a new vertex. As such, a high level of throughput with minimal latency is achieved within the pipeline of the computation engine 110.

If we adopt the narrow interpretation of the Staff and Respondents, it would exclude the preferred embodiments of the '935 patent because even the preferred embodiments may not satisfy the "minimize idle time." Indeed, as the Staff and Respondents argue, "a skilled artisan would understand that it is not technically feasible to order a given set of operation codes in such a way as to truly 'minimize idle time' of a computation engine." (*See* RIMB at 62; SMB at 48 (citing Lastra Decl. at ¶ 30).) But "a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct." *See Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013).

Respondents also question how Complainant AST will be able to prove infringement, arguing that "there's no teaching how to measure idle time." (*See* June 21, 2016 *Markman* Tr. at 303:2-3.) Complainant AST argues that the processing rates of the arbitration module and the computation engine can be compared to prove infringement. (*See id.* at 369:21-370:14.)

Although I am not convinced Complainant AST can satisfy its burden to prove infringement by using "processing rate" as proxy for "idle time," at this time, I do not find clear and convincing evidence that the claim phrase "in an order to minimize the idle time of the computation engine" is indefinite. For the foregoing reasons, and as suggested by the Staff

during the *Markman* hearing, I construe the disputed claim phrase as “in a sequence that minimizes idle time of the computation engine relative to without an application specific prioritization scheme.” (See June 21, 2016 *Markman* Tr. at 383:4-384:25.)

VI. CONCLUSION

The disputed terms of the '428 and '935 patents shall be construed as follows:

Term	Construction
“texture address module”	Plain and ordinary meaning. No construction necessary
“arbitration module”	Plain and ordinary meaning. No construction necessary
“operation code”	Plain and ordinary meaning. No construction necessary
“computation engine”	Plain and ordinary meaning. No construction necessary
“in an order to minimize idle time of the computation engine”	In a sequence that minimizes idle time of the computation engine relative to without an application specific prioritization scheme

SO ORDERED.



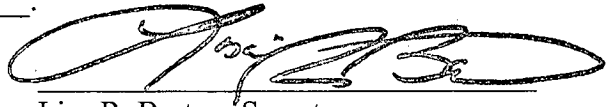
Thomas B. Pender
Administrative Law Judge

**IN THE MATTER OF CERTAIN COMPUTING OR
GRAPHICS SYSTEMS, COMPONENTS THEREOF,
AND VEHICLES CONTAINING SAME**

337-TA-984

CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **PUBLIC ORDER NO. 42** has been served upon the **Commission Investigative Attorney, Jeffrey T. Hsu, Esq.**, and the following parties as indicated on **JULY 15, 2016**.



Lisa R. Barton, Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112A
Washington, DC 20436

FOR COMPLAINANTS ADVANCE SILICON TECHNOLOGIES, LLC.:

Michael T. Renaud, Esq.
MINTZ LEVIN COHN FERRIS GLOVSKY
AND POPEO PC
One Financial Center
Boston, MA 02111

() Via Hand Delivery
() Via Express Delivery
(☒) Via First Class Mail
() Other: _____

**FOR RESPONDENTS HARMAN INTERNATIONAL INDUSTRIES, INC., HARMON
BECKER AUTOMOTIVE SYSTEMS, INC. , HARMAN BECKER AUTOMOTIVE
SYSTEMS GmbH**

Nina S. Tallon, Esq.
WILMER CUTLER PICKERING HALE AND DORR LLP
1875 Pennsylvania Avenue, N.W.
Washington, DC 20006

() Via Hand Delivery
() Via Express Delivery
(☒) Via First Class Mail
() Other: _____

**FOR RESPONDENTS TOYOTA MOTOR CORPORATION, TOYOTA MOTOR
NORTH AMERICA INC., TOYOTA MOTOR SALES, U.S.A., INC.,
TOYOTA MOTOR ENGINEERING & MANUFACTURING NORTH AMERICA, INC.,
TOYOTA MOTOR MANUFACTURING, INDIANA, INC., TOYOTA MOTOR
MANUFACTURING, KENTUCKY, INC., TOYOTA MOTOR MANUFACTURING,
MISSISSIPPI, INC.**

Thomas W. Winland, Esq.
**FINNEGAN, HENDERSON, FARABOW, GARRETT &
DUNNER, L.L.P.**
901 New York Avenue, N.W.
Washington, DC 20001

() Via Hand Delivery
() Via Express Delivery
(☒) Via First Class Mail
() Other: _____

**IN THE MATTER OF CERTAIN COMPUTING OR
GRAPHICS SYSTEMS, COMPONENTS THEREOF,
AND VEHICLES CONTAINING SAME**

337-TA-984

**FOR RESPONDENTS BAYERISCHE MOTEREN WERKE AG, BMW OF NORTH
AMERICA, LLC, BMW MANUFACTURING CO., LLC :**

Joseph P. Lavelle, Esq.
DLA PIPER LLP (US)
500 Eighth Street, N.W.
Washington, DC 20004

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other: _____

**FOR RESPONDENTS FUJITSU TEN LIMITED & FUJITSU TEN CORP. OF
AMERICA, INC., HONDA MOTOR CO., LTD., HONDA NORTH AMERICA, INC.,
AMERICAN HONDA MOTOR CO. INC., HONDA ENGINEERING NORTH
AMERICA, INC., HONDA OF AMERICA MFG., INC., HONDA MANUFACTURING
OF ALABAMA, LLC., HONDA MANUFACTURING OF INDIANA, LLC. & HONDA R
& D AMERICAS, INC.**

G. Brian Busey, Esq.
MORRISON & FOERSTER, LLP
2000 Pennsylvania Avenue N.W., Suite 6000
Washington, DC 20006

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other: _____

FOR RESPONDENT NVIDIA CORPORATION

Maximilian A. Grant, Esq.
LATHAM & WATKINS, LLP
555 Eleventh Street N.W., Suite 1000
Washington, DC 20004

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other: _____

**FOR RESPONDENTS RENESAS ELECTRONICS CORPORATION & RENESAS
ELECTRONICS AMERICA, INC.**

Liane M. Peterson, Esq.
FOLEY & LARDNER, LLP
3000 K Street N.W., Suite 600
Washington, DC 20007

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other: _____

FOR RESPONDENT TEXAS INSTRUMENTS INC.

Sturgis M. Sobin, Esq.
COVINGTON & BURLING, LLP
One CityCenter
850 Tenth Street, N.W.
Washington, DC 20001

☐ Via Hand Delivery
☐ Via Express Delivery
☒ Via First Class Mail
☐ Other: _____

**IN THE MATTER OF CERTAIN COMPUTING OR
GRAPHICS SYSTEMS, COMPONENTS THEREOF,
AND VEHICLES CONTAINING SAME**

337-TA-984

**FOR RESPONDENTS VOLKSWAGEN AG, VOLKSWAGEN GROUP OF AMERICA,
INC., VOLKSWAGEN GROUP OF AMERICA, CHATTANOOGA OPERATIONS,
LLC., AUDI AG & AUDI OF AMERICA, LLC.**

Daniel E. Yonan, Esq
STERNE, KESSLER GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue N.W.
Washington, DC 20005

() Via Hand Delivery
() Via Express Delivery
(☒) Via First Class Mail
() Other: _____