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UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

2010-1176

TESSERA, INC.,

Appellant,

v.

INTERNATIONAL TRADE COMMISSION,

Appellee.

and

ELPIDA MEMORY, INC. and ELPIDA MEMORY (USA) INC.,

Intervenors,

and

SMART MODULAR TECHNOLOGIES, INC.,

Intervenors,

and

ACER, INC., ACER AMERICA CORPORATION, NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., and POWERCHIP SEMICONDUCTOR CORPORATION,

Intervenors,

and

RAMAXEL TECHNOLOGY LTD.,

Intervenors,

and

KINGSTON TECHNOLOGY COMPANY, INC.,

Intervenors.

On appeal from the United States International Trade Commission in
Investigation No. 337-TA-630.

BRIEF OF INTERVENOR KINGSTON TECHNOLOGY COMPANY, INC.

FILED
U.S. COURT OF APPEALS FOR
THE FEDERAL CIRCUIT

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CERTIFICATE OF INTEREST

Pursuant to Fed. Cir. R. 27(a)(7) and 47.4, counsel for Kingston Technology Company, Inc. certify the following:

1. The full name of every party or amicus represented by me is: **Kingston Technology Company, Inc.**
2. The name of the real party in interest represented by me is: **Same as above.**
3. All parent corporations and any publicly held companies that own 10% or more of the stock of the party or amicus curiae represented by me are: **Kingston Technology Corporation**
4. The names of all law firms and partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

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*: no longer with the firm

DATED: July 20, 2010

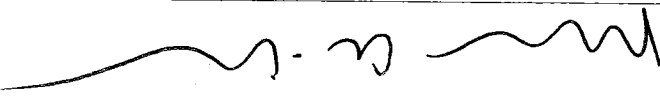

Matthew A. Werber

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CONFIDENTIAL MATERIAL OMITTED

The material omitted on pages ii, 2, 10-13, 15-18, 28 and 31-32 provides

certain technical details concerning the DRAM package assemblies at issue in this

action and the manner in which they are packaged. A vendor who sources the

accused DRAM packages to Kingston advised Kingston that it is their position that

these technical details are confidential and should be redacted in the

nonconfidential version of this brief.

The material omitted on pages 14 and 25-26 discloses testimony taken at an

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STATEMENT OF RELATED CASES

Appellant Tessera, Inc. appeals a Final Determination of the United States

International Trade Commission ("ITC" or "Commission"), in which the

Commission determined intervenor Kingston Technology Company, Inc.

("Kingston") and the other Respondents have not violated section 337 of the Tariff

Act of 1930 (19 U.S.C. § 1337) because Respondents do not infringe the asserted

claims of United States Patent Nos. 5,663,106 ("the '106 patent"), United States

Patent No. 5,679,977 ("the '977 patent") and United States Patent No. 6,133,627

("the '627 patent").

The '977 and '627 patents are related to U.S. Patent Nos. 5,852,326 and

6,433,419. U.S. Patent No. 5,663,106 incorporates by reference U.S. Patent No.

5,148,265, which is the parent of the '326, and '419 Patents.

The '326 and '419 patents are at issue in *Spanston, Inc. v. Commission*, Nos.

09-1460, 1461, 1462 & 1465, currently pending before this Court.

One or more patents at issue here are at issue in pending district court cases,

including: *Tessera, Inc. v. A DATA Technology Co.*, 2:07 CV 534 (E.D.Tex.);

Tessera, Inc. v. Advanced Micro Devices, Inc., C05 04063 CW (N.D.Cal.);

Siliconware Precision Industries Co. et al. v. Tessera, Inc., No. C08 03667 CW

(N.D.Cal.); *ChipMOS Technologies Inc. v. Tessera, Inc.*, No. C08 03827 CW

(N.D.Cal.); and *Advanced Semiconductor Engineering Inc. et al. v. Tessera, Inc.* No. C08 03726 CW (N.D.Cal.). All of these cases are presently stayed.

The '106 patent is at issue in *Powertech Technology Inc. v. Tessera, Inc.*,

CV 10-009945 CW (N.D. Cal.). In that case, Plaintiff Powertech Technology Inc.

has filed a motion for reconsideration of an order of dismissal issued by the district

court.

The '977 patent is presently undergoing reexamination before the United

States Patent and Trademark Office as part of reexamination control nos.

90/008,484, 90/008,528, and 90/008,695. The '627 patent is presently undergoing

reexamination as part of reexamination control nos. 90/008,485, 90/008,696, and

90/009,096. The '106 patent is presently undergoing reexamination as part of

reexamination control no. 90/009,215.

STATEMENT OF JURISDICTION

Tessera contends the Commission's determinations are reviewable under 28 U.S.C. § 1295(a)(6). Kingston agrees with that contention, but only in part.

Particularly, this Court does not have jurisdiction over the Commission's October 30, 2009 determination that accused products purchased from or assembled by Tessera licensees are subject to patent exhaustion and, therefore cannot infringe.

(JA51-53).

Pursuant to Fed. R. App. P. 4(a)(1)(B), Tessera was required to appeal that issue within "60 days" after the October 30, 2009 determination by the

Commission. Tessera, however, did not file a notice of appeal until January 28, 2010 -- several weeks beyond the 60-day deadline. Thus, Tessera's appeal of the Commission's determination on patent exhaustion should be dismissed as

untimely. This issue is discussed in detail in the Commission's brief, which

Kingston joins herein.

STATEMENT OF ISSUES

1. Is there substantial evidence in the record to support the

Commission's finding that the



*2. Is the Commission's finding that the solder mask is not part of the

claimed "top layer" of claim 1 a finding on claim construction, and, if so, do the

fundamental tenets of claim construction support that finding?

3. Should Tessera's appeal of the Commission's October 30, 2009

determination on patent exhaustion be dismissed as untimely under Fed. R. App. P.

4(a)(1)(B) -- which requires a notice of appeal within "60 days" -- when Tessera

waited until January 28, 2010 (several weeks beyond the 60-day deadline) to file

its notice of appeal regarding this issue?

4. Did the Commission correctly conclude that all packages at issue

purchased from or assembled by Tessera licensees are subject to patent exhaustion

because the license agreements unconditionally authorize the licensees to make,

use, and sell such packages?

* Kingston focuses on Issue No. 2 in this brief. The remaining issues are

addressed in detail in the Acer-Nanya-Powertip ("ANP"), Elpida and

Commission briefs, which Kingston joins and incorporates herein.

STATEMENT OF THE CASE

Tessera, Inc. ("Tessera") named Kingston and seventeen other companies as

Respondents in a complaint filed with the United States International Trade

Commission ("ITC" or "Commission") in December 2007. Tessera alleged

Respondents violated section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) by

infringing claims of several U.S. patents. After reviewing Tessera's Complaint,

the Commission initiated Investigation No. 337-TA-630 (the "Investigation").

In response to the Complaint, Kingston denied it infringed the claims of the

asserted patents and raised defenses of patent exhaustion, license, equitable

estoppel and patent invalidity, among others.

On August 28, 2009, the Administrative Law Judge ("ALJ") issued a final

Initial Determination ("ID"), which found Respondents do not violate section 337

with respect to any of the asserted patent claims. JA54-235. Particularly, the ALJ

found that all accused packages at issue (both WBGA and µBGA packages) do not

infringe the asserted claims of the '106 patent and that all packages purchased from

or assembled by Tessera licensees were authorized to be sold by Tessera and, thus,

Tessera's rights in those chips became subject to exhaustion. JA112-13; JA210.

On October 30, 2009, the Commission determined to review the final ID, but

only in-part. JA50-51. Significantly, the Commission determined to not review

the ID's determination regarding Respondents' patent exhaustion defense.

On January 4, 2010, the Commission issued its Final Determination opinion. 2010 WL 686377 (U.S.I.T.C. Feb. 24, 2010)(JA144) (“Comm’n Opinion”). In the Final Determination, the Commission, in relevant part: (1) modified the ALJ’s

construction of the claim terms “top layer” and “thereon” recited in claim 1 of the ‘106 patent; (2) affirmed the ALJ’s finding that Respondents’ wBGA products do not infringe the ‘106 patent; and (3) affirmed the ALJ’s finding that Respondents do not infringe the ‘977 and ‘627 patents.

Tessera filed its opening appeal brief May 27, 2010. In that brief, Tessera contends the Commission erred when it determined Respondents wBGA packages do not infringe the asserted claims of the ‘106 patent, but did not address the Commission’s determination as to the ‘977 and ‘627 patents.

Tessera’s opening brief also discusses the Commission’s October 30, 2009 determination that accused products purchased from or assembled by Tessera

licensees are subject to patent exhaustion and, therefore, cannot infringe. Yet, as set forth in the jurisdiction section above, Tessera’s attempt to now bring that issue into this appeal is untimely and, therefore, is not subject to review by this court.

STATEMENT OF THE FACTS

I. The accused Kingston memory products.

Kingston -- based in Fountain Valley, California -- is a designer and manufacturer of many different types of memory products, including dynamic random access memory ("DRAM") memory modules. (JA168600, JA168618 - JA168619). Kingston does not make or sell the DRAM chip packages Tessera contends are covered by the claims of the asserted patents. (JA168627 - JA0168629). Instead, Kingston purchases DRAM chip packages from outside vendors -- many of which are Tessera licensees -- in order to make and sell memory "modules," which comprise multiple DRAM chip packages mounted on a circuit board. (JA168627 - JA0168629); (JA0164091).

In this case, Tessera has accused two types of DRAM packages: (1) "window Ball Grid Array ("BGA") packages; and (2) "micro Ball Grid Array" (µBGA) packages. (Opening Brief of Appellant Tessera "T. Br." at 6). Tessera's infringement allegations against Kingston, however, concern only BGA packages. (JA29). Thus, Kingston discusses only BGA packages in this brief.

II. The '106 patent.

Semiconductor chip assemblies contain many delicate components,

including the chip itself and other electrical circuitry. (JA63929). Thus, it is

common to apply an "encapsulant" (i.e. molded plastic material or the like) around

those delicate components in order to protect them from damage. *Id.* When

introducing the encapsulant, the manufacturer must keep the encapsulant away

from the "terminals," which permit the semiconductor chip assembly to be

electrically connected to other components of an electronic product that uses the

semiconductor chip assembly. JA63948. Otherwise, the semiconductor chip

assembly would be unable to function because its terminals would be essentially

sealed off from the remainder of the product being manufactured. *Id.*

The '106 patent is directed to a method for introducing encapsulant (a/k/a

molding compound) into a semiconductor chip assembly and, more specifically, to

a method for preventing the encapsulant from contaminating "exposed terminals"

on the top layer of the semiconductor chip assembly. (JA113285).

A. The '106 patent specification.

Referring to Fig. 1 of the '106 patent, depicted below, the '106 patent

discloses a semiconductor chip assembly 10 having a chip 12, elastomeric pad 20,

¹ Kingston discusses only the '106 patent in this brief because Tessera chose not to brief the ITC's noninfringement finding with regard to the other two asserted patents. (T. Br. at 48-49).

and "top layer" 16 with an array of exposed terminals 26 fixed on that top layer 16. (JA113280, Fig. 1); (JA113287 at Col. 5, Lns. 8-35). During the encapsulation

process, the semiconductor chip assembly 10 is placed inside an "encapsulant

barrier," which at least partially forms an encapsulation area. *Id.* In this

embodiment, the encapsulant barrier is an aluminum can 28. *Id.* The "protective

barrier" (in this embodiment, a solder mask 30) is provided to protect the exposed

terminals 26 on the top layer 26 during the encapsulation process. *Id.*; (JA113285

at Col. 2, Lns. 24-27)).

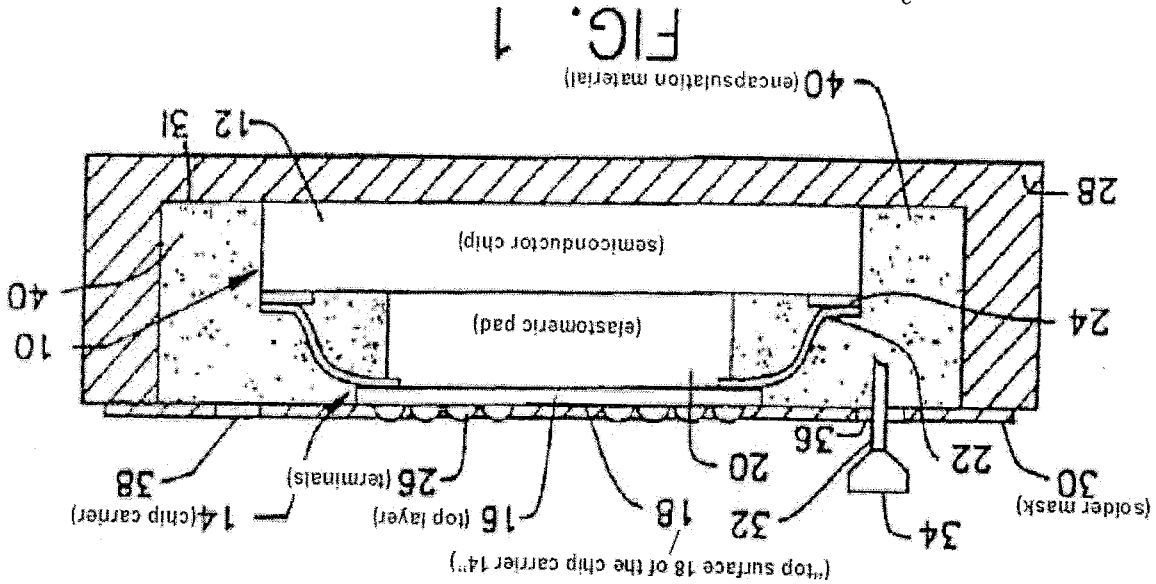


FIG. 1

(JA113280, Fig. 1).² When the encapsulation material 40 is introduced into the encapsulation area through a needle 32 or the like, the protective barrier

(corresponding to the solder mask 30 in Fig. 1) prevents the encapsulation material

² Annotations (highlighted in red) have been added to Fig. 1 above for purposes of this brief.

40 from contaminating the exposed terminals 26. (JA113287 at Col. 6, Lns. 5-12).

The specification describes this process as follows:

Once the semiconductor chip assembly 10 has been positioned within the can 28, and the solder mask 30 has been secured to protect the terminals 26 from the encapsulation material, the encapsulation material can be introduced into the encapsulation area, which, in most instances, about the periphery of the semiconductor chip assembly 10. This can be accomplished in a number of ways, including most preferably, the use of a needle 32 which is connected to a source 34.

(JA113287 at Col. 6, Lns. 5-14) (emphasis added).

The '106 patent specification teaches that if a solder mask is used as a

protective barrier, the solder mask would be placed in contact with (and,

preferably, vacuum laminated to) the top layer. (JA113288, Col. 7, Lns. 39 - 43);

(JA113285, Col. 2, Lns. 36 - 39).³

Referring to Fig. 4 (shown below), the '106 patent depicts a solder mask

having an "array of terminal holes 37" to be "pressed over the terminals 26," so the terminals 26 (which are fixed on the top layer) can be exposed for electrical connection. (JA113287, Col. 5, Lns. 45 - 56) (emphasis added) (JA113281, Fig. 4).

In particular, the '106 patent specification states:

While the solder mask 30 could merely have a large opening through which the array of terminals 26 are exposed, the solder mask 30 being connected to the perimeter of the top surface of chip carrier 14, it

³ As Tessera explains, the '106 patent specification incorporates the specifications of two other patents by reference -- namely U.S. Patent Nos. 5,148,265 and 5,477,611. The '265 and '611 patents, however, do not disclose use of a solder mask.

is preferable to provide solder mask 30 with an array of terminal holes corresponding to the array of terminals 26 on the chip carrier 14. The array of terminal holes 37 is shown clearly in FIG. 4. The terminal holes 37 can be registered with the terminals 26, and are preferably of such a size that the solder mask 30 must be pressed over the terminals 26. This provides a relatively tight fit of the terminals 26 in the terminal holes of the solder mask 30.

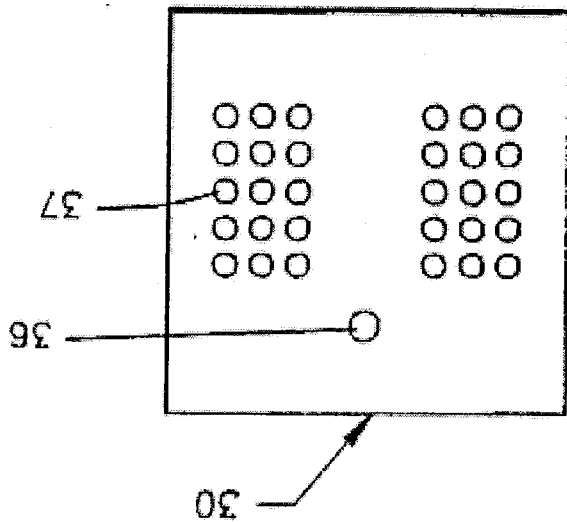


FIG. 4

(JA113287, Col. 5, Lns. 45 - 56) (emphasis added); (JA113281, Fig. 4).

B. Claim 1 of the '106 patent.

Method claim 1 -- the only independent claim at issue here -- reads as

follows, with certain relevant claim language highlighted in bold:

A method of encapsulating a semiconductor chip assembly having a **top layer with an array of exposed terminals thereon**, the terminals being electrically connected to the chip, said method comprising the steps of:

placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulation area;

providing a protective barrier in contact with said top layer for protecting the terminals on the top layer from an encapsulation material; and

introducing an encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition, the protective barrier preventing the encapsulation material from contacting the terminals on the top layer.

(JA113239, claim 1) (*emphasis added*).

C. The Commission's Final Determination.

In its Final Determination ("JA"), the Commission concluded that the

encapsulation method used for Respondents' accused WBGA packages does not

infringe method claim 1 of the '106 patent.⁴ For these accused WBGA packages,

the Commission determined that

A description of the

Commission's analysis with reference to Fig. A to this brief is set forth below.⁵

⁴ The ITC found that the accused μ BGA packages (asserted only against Elpida) meet each limitation of claim 1, but found that Elpida's μ BGA packages do not infringe because they are subject to the patent exhaustion defense. (JA28). The Commission's analysis regarding μ BGA packages is inapplicable to the WBGA packages discussed in this brief because the structures of these two packages are different. For example,

⁵ Fig. A of this brief is a graphic Tessera provided in its opening brief to depict the basic components of Respondents' accused WBGA packages and the molding process used for those packages. Annotations (highlighted in red) have been added for purposes of this brief.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

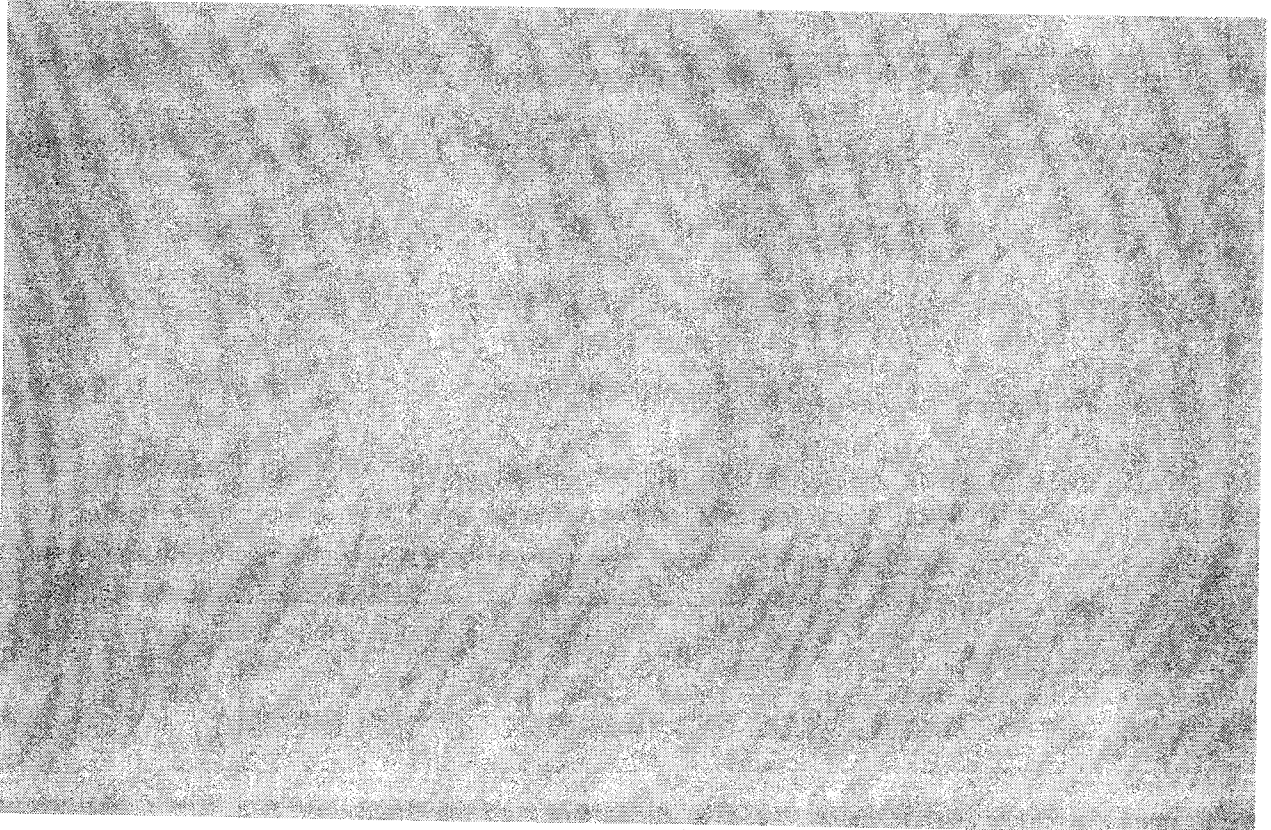
[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Referring to Fig. A above, the Commission determined (by adopting the

ALJ's finding) that



[REDACTED]



principles of claim construction, the Court would find that [REDACTED]

construction. Tessera also asserts that if this Court were to properly apply the characterization of the Commission's analysis on this issue as a ruling on claim [REDACTED] and [REDACTED]

Tessera contends that the Commission erred when [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

construing the term "top layer," the Commission: [REDACTED]

with [a] top layer" of a semiconductor chip assembly. (JA113289). After '106 patent. Claim 1 recites the step of "providing a protective barrier in contact for Respondents' accused wBGA packages does not infringe method claim 1 of the

The Commission correctly determined that the encapsulation method used

SUMMARY OF ARGUMENT

not infringe method claim 1 of the '106 patent.

the encapsulation method used for Respondents' accused wBGA packages does

For these reasons, the Commission concluded that [REDACTED]

As set forth herein,

Tessera's argument fails.

As a threshold matter, the Commission's conclusion that the

[REDACTED] This issue is discussed in detail in the Acer-Nanya-

Powerchip ("ANP"), Elpida and Commission briefs, which Kingston joins and

incorporates herein. As discussed in these briefs, the Commission's determination

is supported by "substantial evidence" and, therefore, should not be overturned.

Should the Court, however, agree with Tessera that the Commission's

noninfringement finding is a finding regarding claim construction, the

Commission's ruling should nevertheless stand, because the Commission's finding

that

For example, the intrinsic evidence of the '106 patent unmistakably

demonstrates that a person of ordinary skill in the art would understand that a

solder mask, if used, is completely separate from the claimed "top layer" of claim

1. Further, the '106 patent specification makes clear that a solder mask bears no

relation to a structure -- such as the "top layer" -- which is required by claim 1 to

have terminals disposed "thereon" the top layer. The solder mask is consistently disclosed as having openings or holes through which the terminals disposed on the "top layer" may be "exposed" -- which is completely different from a structure which has terminals located "thereon," as claim 1 requires for the top layer. Indeed, Dr. DiStefano -- Tessera's founder and one of the '106 patent inventors -- testified at trial that that

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

Tessera also contends that the Commission improperly limited the scope of

claim 1 to a preferred embodiment disclosed in the '106 patent specification. (T.

Br. at 27). This is not true. The Commission never found (and Respondents are

not contending) that claim 1 must be limited to any embodiment disclosed in the

'106 patent specification. Instead, the Commission's finding merely recognizes

that one of ordinary skill in the art reading the '106 patent would conclude that if a

solder mask is used, that solder mask would be a separate component from the "top

layer" and could not be part of it.

Tellingly, Tessera has cited to no evidence to the contrary, outside of its

contention that the '106 patent does not contain language expressly excluding a

solder mask from the claimed "top layer." The rules of claim construction,

however, do not permit Tessera, without evidentiary support, to pick and choose from virtually any combination of structures as corresponding to the claimed "top layer." Instead, the rules of claim construction, when applied properly, lead to the inescapable conclusion that a solder mask is separate from the claimed "top layer" and cannot be part of it.

ARGUMENT

In addition to the arguments and positions set forth in the Acer-Nanya-Powerchip ("ANP"), Elpida and Commission briefs -- which Kingston joins and incorporates herein -- Kingston provides the following additional arguments and positions showing why the Commission was correct in concluding that Respondents' accused BGA packages do not infringe the asserted independent claim 1 of United States Patent No. 5,633,106 (the "'106 patent").

The Commission concluded that the encapsulation method used for Respondents' accused BGA packages does not infringe method claim 1 of the '106 patent. For these accused BGA packages, the Commission determined that

