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No. 2010-1270

IN THE
UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

QIMONDA AG,
Appellant,

FILED
U.S. COURT OF APPEALS FOR
THE FEDERAL CIRCUIT
JUL 2 6 2010

v.

INTERNATIONAL TRADE COMMISSION,
Appellee,

JAN HORBALY
CLERK

and

LSI CORPORATION,
Intervenor,

and

SEAGATE TECHNOLOGY, SEAGATE TECHNOLOGY (US) HOLDINGS INC., SEAGATE TECHNOLOGY LLC, and SEAGATE (US) LLC.,
Intervenors.

On appeal from the United States International Trade Commission
in Investigation No. 337-TA-665

CORRECTED NON-CONFIDENTIAL BRIEF OF APPELLANT QIMONDA AG

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Dated: July 26, 2010

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CERTIFICATE OF INTEREST

Pursuant to Federal Circuit Rule 47.4(a)(1) and Federal Rule of Appellate Procedure 26.1, counsel for Qimonda AG certifies the following:

1. The full name of every party represented by me is:

Qimonda AG

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

The parties named in the caption are the real parties in interest.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party represented by me are:

Infineon Technologies AG holds 28.44% of QAG's share capital and Infineon Technologies Investment BV, a wholly-owned subsidiary of Infineon Technologies AG, holds 49,03% of QAG's share capital. To the best of my knowledge, no other corporation owns 10% or more of QAG's equity interests.

4. The names of all law firms and partners or associates that appeared in the agency for the party represented by me or are expected to appear in this court are:

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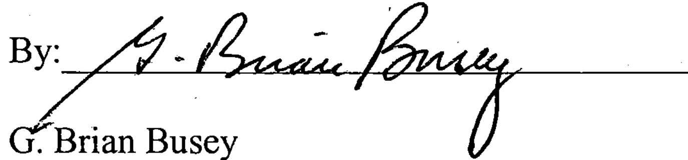
By: 

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Confidential Material Omitted From Public Version
The Confidential Version Of The Appeal Brief Contains Information Concerning The Manufacture And Structure Of The Accused And Domestic Industry Products Subject To The Protective Order Issued In The United States International Trade Commission ("ITC") Investigation Below. The Confidential Version Also Contains Statements From Briefs Subject To The ITC Protective Order. This Material Has Been Redacted From The Public Version. Additionally, The Addendum To The Public Version Of This Brief Contains The Public Version Of The Final Initial Determination Issued By The ITC, In Which Information Subject To The ITC's Protective Order Has Been Redacted By The ITC.

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STATEMENT OF RELATED CASES

The patent at issue in this appeal is also being asserted in *Qimonda AG v. LSI Corp.*, C.A. No. 3:08-cv-00735-JRS (E.D. Va.). That case has been stayed pending the ultimate resolution of this case. *See* 28 U.S.C. § 1659.

JURISDICTIONAL STATEMENT

On January 29, 2010, the United States International Trade Commission ("ITC" or "Commission") invoked jurisdiction under Section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, and rendered a determination that Intervenors LSI and Seagate had not violated Section 337. This appeal was timely filed on March 26, 2010, and this Court has jurisdiction under 19 U.S.C. § 1337(c) and 28 U.S.C. § 1295(a)(6).

STATEMENT OF THE ISSUES

1. Whether the Commission erroneously construed "removing the exposed portion of the insulating material over the active regions" – which is part of the etching step for "removing at least a portion of the insulating material covering the active regions" in the '899 patent – to require that *all* insulating material over the active regions be removed, when the claim language, specification, and prosecution history all demonstrate that only a portion of that insulating material must be removed at the etching step.

2. Whether, under the correct construction of "removing the exposed portion of the insulating material over the active regions," the Commission erred in finding that the processes used to fabricate the accused products do not infringe the '899 patent; and

3. Whether, under the correct construction of "removing the exposed portion of the insulating material over the active regions," the Commission erred in finding that the process used to fabricate Qimonda's domestic industry product does not practice the '899 patent.

STATEMENT OF THE CASE

A. Nature Of The Case

This appeal involves the ITC's determinations that Intervenors LSI Corporation ("LSI") and Seagate Technology, Seagate Technology (US) Holdings, Inc., Seagate Technology LLC, Seagate Memory Products (US) Corporation, and Seagate (US) (collectively, "Seagate") did not violate 19 U.S.C. §1337 ("Section 337") by importing into the United States, selling for importation into the United States, or selling after importation into the United States products that infringe the '899 patent. The ITC's determination that LSI and Seagate did not violate Section 337 with respect to '899 patent is based entirely on a single erroneous claim construction.

B. Course Of Proceedings

On November 20, 2008, Appellant Qimonda filed a complaint with the ITC alleging that Intervenors LSI and Seagate violated Section 337 by importing, selling for importation, or selling after importation chips that infringed seven patents, including U.S. Patent No. 5,851,899 (the '899 patent), and products containing such chips. (A2893-A2944.) On December 17, 2008, in response to

Qimonda's complaint, the Commission issued a Notice of Investigation. (A1062-A1063.)

At the hearing held from June 1, 2009 to June 9, 2009, Qimonda asserted four patents, including the '899 patent. On October 14, 2009, the presiding Administrative Law Judge ("ALJ") issued a final initial determination on violation ("ID") finding no violation with respect to any of the patents. (A5-A9; A10-A637.)

On October 27, 2009, Qimonda filed a petition for review of the ALJ's finding of no violation with respect to the '899 patent and two other patents. (A2945-A3070.) The Office of Unfair Importation Investigation, LSI, and Seagate did not petition for review of any portion of the ALJ's initial determination. On January 29, 2010, the Commission issued its determination not to review the ALJ's finding regarding the '899 patent. (A1-A4.)

STATEMENT OF THE FACTS

A. Factual Background

1. The technology at issue

The technology at issue in this case relates to the design and fabrication of semiconductor integrated circuits – more commonly known as chips. The '899 patent covers their design and manufacture.

A chip is a circuit that has been manufactured on the surface of a thin substrate of semiconductor material, most often a silicon wafer. Fabrication of a

chip often involves hundreds of precise processing steps, and is complex and time consuming. Several hundreds, even thousands, of identical chips are fabricated at once on the surface of a single silicon wafer. The chips are tested and then separated from each other for further processing. (A2240-A2241 at Q&A 40-45.)

Because each semiconductor integrated circuit comprises many overlapping layers, the manufacturing process ordinarily begins at the bottom of a chip with a base substrate layer – a silicon wafer – and proceeds upwards. Active devices, such as transistors, are created in and on the silicon wafer. These active devices are separated from each other by isolation structures, including shallow isolation trenches which create a barrier between the active structures on each level to avoid electrical current leakage. On top of that level is a layer of silicon dioxide, commonly abbreviated as "oxide," which provides insulation between each active level of the chip. Thus, in a single chip, there are several active substrate layers, with active devices that provide electrical connections inside and outside the chip, along with intervening oxide layers that provide insulation between the levels. (A2241 at Q&A 46-49.)

2. *U.S. Patent No. 5,851,899*

a. Qimonda is a publicly traded company with its corporate headquarters in Munich, Germany. (A2578.) Qimonda designs and manufactures semiconductor memory technologies. (A2693.) Qimonda also invests significant

money each year on research and development and the protection of its intellectual property rights. (A2700.) At the time of the filing of the complaint, Qimonda operated a research and development center in Cary, North Carolina, A2387; A2753, and was one of the largest suppliers of dynamic random access memory (DRAM) products in the world, A2384-A2385. Today, Qimonda is subject to insolvency proceedings under German law.[1]

At the time the ITC case was filed, Qimonda's operations in the United States were overseen by its wholly owned subsidiary, Qimonda North America. (A2384; A2799.) Qimonda Richmond was a wholly owned subsidiary of Qimonda North America located at Sandston, Virginia, just outside of Richmond. (A2384; A2799.) Qimonda Richmond managed Qimonda's two United States based DRAM semiconductor manufacturing and testing facilities in Richmond, Virginia. (A2711; A2718.) Qimonda also operated a sales and marketing office in San Jose, California. (A2387; A2753.)

Qimonda owns by assignment the entire right, title, and interest in the '899 patent.

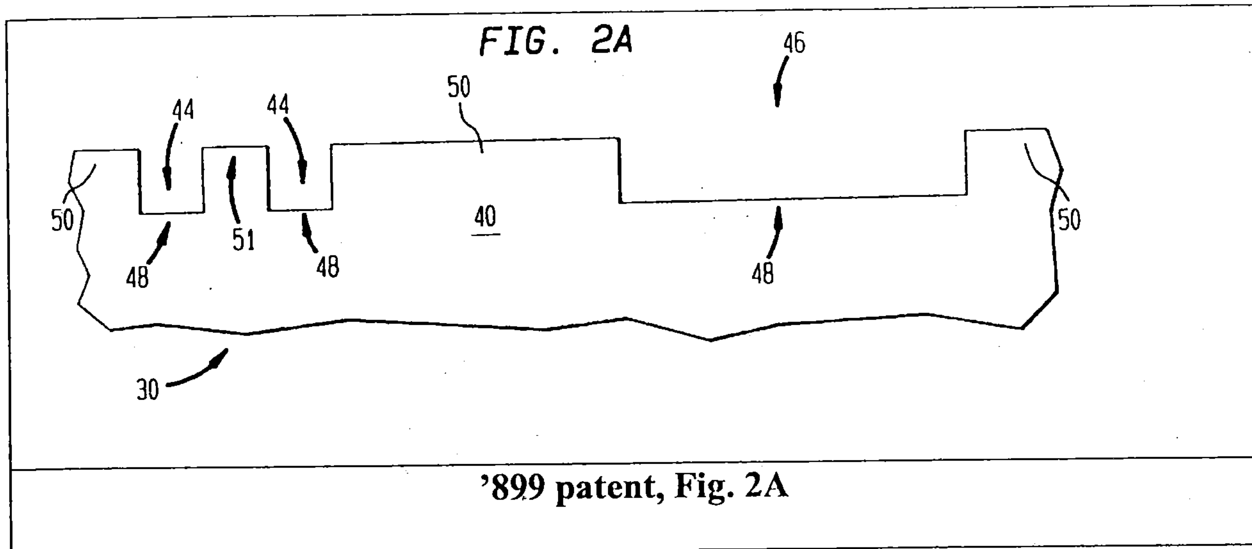
---

[1] On January 23, 2009, Qimonda AG filed for insolvency under German law. (A2390.) And on February 20, 2009, QNA and QR filed for creditor protection in Delaware under Chapter 11 of the U.S. Bankruptcy Code and are currently reorganizing through Chapter 11 bankruptcy. (A2353-A2380; A2381-A2420.)

b. *The background of the invention.* The '899 patent is directed to the construction of semiconductor integrated circuits. As the size of these chips has been reduced, the various active components on each level of a chip must be positioned closer together. This, in turn, requires effective isolation structures because, when active components are formed near each other, electrical current leakage between them can occur and cause malfunctions. (A2245 at Q&A 69.)

Shallow trench isolation provides the necessary insulation between the active components on a single layer of substrate. During the early stages of fabrication, trenches are etched into the substrate. These trenches – called "shallow trench isolation regions" (STI regions) – delineate the various active regions on the chip. (A679 at col. 1:24-26). An active region is where on the substrate an active component will be formed.

To form STI regions, an etching mask is placed over the substrate. The pattern of the etching mask determines the pattern of trenches. The portions of the substrate not overlain with photoresist (material that prevents etching) are etched to form trenches, whereas the areas overlain by photoresist are not etched and form the active regions. Figure 2A of the '899 patent depicts the cross-section of a substrate with active regions (50, 51) separated by trenches (44, 46):

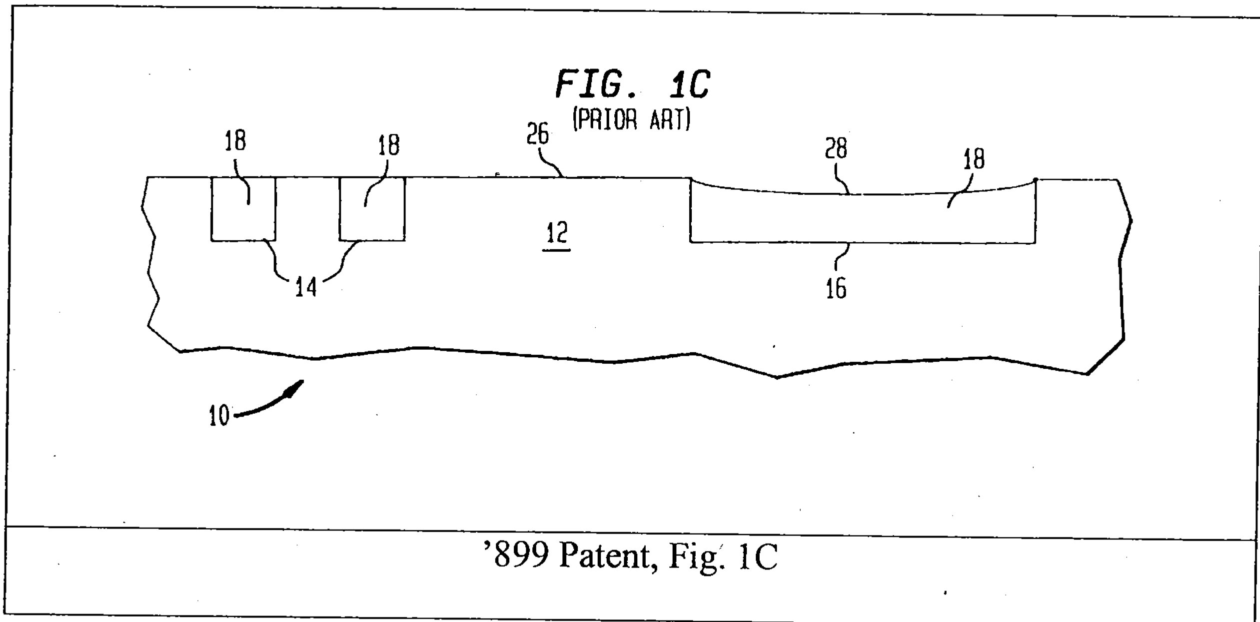


'899 patent, Fig. 2A

To isolate the active components that will be formed on the active regions (to prevent electrical current leakage), the trenches are filled with an insulating material such as oxide. (A2245-A2248 at Q&A 67-86; A2288 at Q&A 50.) This is accomplished by coating the entire substrate level – trenches and active regions alike – with the insulating material. (A679 at col. 1:19-24). The insulating material is deposited so that it fills the STI regions without any leaving any gaps. (A681 at col. 5:25-26.) One of the methods that allow the insulating material to be so deposited is high density plasma source deposition ("HDP-CVD"). (*Id.*)

After oxide has been deposited, both the active regions and shallow trenches are entirely coated with oxide and the surface of the insulating material is irregular and uneven. Because a chip is composed of many layers on top of one another, it is necessary to "planarize" – i.e., smooth – the excess insulating material on the chip, so that its surface is flat and even. (A679 at col. 1:57-63).

This planarizing step is typically performed by chemical mechanical polishing ("CMP"). As was known in the prior art, however, a long CMP step can result in too much insulating material being removed from the STI regions, resulting in "dishing" as depicted in Figure 1C of the '899 patent.



'899 Patent, Fig. 1C

As the background of the invention explains:

> Long CMP steps, for example, have been known to cause oxide erosion, especially in the widest of STIs. As can be seen in FIG. 1C, during STI planarization using a long CMP planarization step, the erosion of oxide, particularly in the wide STI 16, poses a major problem. The surface of the oxide layer 18 is not planar, dipping below the surface 26 of the semiconductor substrate 12 and resulting in an uneven topography. This phenomenon is especially pronounced at the center 28 of the oxide layer 18 in the wide STI 16.

(A679 at col. 2:51-60.)

The duration of the CMP step is dependent on the amount of insulating material that needs to be removed. Not surprisingly, the more insulating material

that needs to be removed, the longer the CMP step. Because the active areas of a given integrated circuit can be of any size and located in any position on the substrate, shallow trenches typically vary widely in dimension, (A679 at col. 1), and wider shallow trenches become more prone to dishing during the CMP process, (*id.* at col. 2).

A number of complex processes were known in the prior art to solve the problem of providing a highly planarized integrated circuit structure without dishing. Many of these methods, however, require additional processing steps, which reduce efficiency while adding cost to the overall manufacturing process. (A679 at col. 3.)

c. *The invention.* The '899 patent claims a method to remove the excess insulation material that is formed on the chip during the creation of isolation structures. The '899 patent significantly simplifies this process over the prior art, using a minimum amount of process steps and equipment, while achieving superior planarization of the insulation material.

At the heart of the invention, the inventors of the '899 patent came up with a simple way to generate and use an etching mask in removing a portion of the excess insulating material on top of the active regions prior to planarization. This process – the generation and use of an etching mask for the etching step –

simplifies the manufacturing process and reduces the amount of time the CMP process must be used during planarization.

By using the *inverse* of the etching mask that was used to create the shallow trenches, the pattern of photoresist (i.e., the protective material that prevents etching) is placed on top of the oxide deposited in the shallow trenches. The photoresist layer in the etching mask thus protects the oxide beneath it (covering the shallow trenches) from being etched away. And, in order to ensure that the STI regions are fully protected from etching, as Figure 4A shows, the '899 patent teaches that the inverse etching mask can be biased so that the photoresist (60) covering the STI regions (52) overlaps the edges of the active regions (50, 51).

FIG. 4A

'899 patent, Fig. 4A

Once the inverse etching mask is placed, as claim 1 of the '899 patent recites, "at least a portion of the insulating material covering the active regions" is removed

during the etching step. After that, during the planarization step, the chip surface is planarized to "expose the active regions."[2]

The use of a biased, inverse etching mask covering the STI regions is the novel and allowable subject matter of the '899 patent.

d. *Prosecution history.* The application that led to the '899 patent contained a single method claim for "forming isolation between device structures fabricated on a substrate." (A704.) Application claim 1 required the planarization of insulating material deposited by HDP-CVD, but did not require a portion of the

[2] Claim 1 of the '899 patent recites in relevant part:

> [the etching step as] removing at least a portion of the insulating material covering the active regions; and
>
> [the planarization step as] planarizing the surface of said substrate to expose the active regions, the removal of at least a portion of insulating material from the active regions providing a planar topography; wherein removing of at least a portion of the insulating material from the active regions includes:
>
> depositing a mask layer over the insulating material;
>
> patterning the mask layer to expose at least a portion of the insulating material over the active regions; and
>
> removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials; and wherein the mask layer is deposited using an inverse active area mark that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions.

excess insulating material be removed prior to the planarizing step. (*Id.*) The patent examiner rejected the application as anticipated by prior art disclosing the use of a planarization step on insulating material deposited by HDP-CVD. ('899 Pros. His., Office Action (Jun. 18, 1997) at A778-A780.)

In response to the rejection, the applicants amended claim 1 and submitted 37 new application claims. Amended application claim 1 required that a portion of the insulating material deposited over the active areas be removed before the planarizing step. ('899 Pros. His., Response (Nov. 18) at A800-A801.) Amended application claim 1 did not require, however, that this insulating material be removed in any particular way. (*Id.*) By contrast, some application claims specified that this material was to be removed through etching (application claims 5, 17, 29) without specifying how the etching mask was to be formed, while other application claims specified that the etching mask used in the etching step should be an "inverse active area mask" biased so as to overlap portions of the active regions (application claims 6-2, 18-24, 30-38). ('899 Pros. His., Response (Nov. 18) at A800-A808.)

In response, the patent examiner issued an office action finding that the claims which included the requirement that the etching step be performed using a biased, inversed etching mask where the photoresist pattern protected the insulation-filled STI regions were either allowable as written or could be allowable

if written in independent form. ('899 Pros. His., Office Action (Mar. 23, 1998) at A815-A817.) The patent examiner rejected the remaining application claims. The applicants withdrew the rejected claims and resubmitted amended claims complying with the patent examiner's findings of allowability. In allowing the amended claims, the patent examiner explained:

> Confidential Material Redacted
>
> Prior art of record does not teach or suggest the claimed invention in which an inverse active area mask is used to remove at least a portion of the insulating layer from the active regions as claimed.

('899 Pros. His., Notice of Allowability (Aug. 03, 1998) at A880.)

3. *The accused products*

The accused products are chips manufactured by LSI using the G12, Gflx, and AL13 processes and downstream products containing those chips, sold or imported by LSI and Seagate. There is no dispute concerning the steps employed by these processes.

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REDACTED

B. Proceedings Below

1. In response to a complaint filed by Qimonda, the ITC instituted an investigation to determine whether LSI and Seagate violated Section 337 by importing into the United States, selling for importation, or the selling within the United States after importation articles that infringe U.S. Patent Nos. 5,213,670 ("the '670 patent"); 5,646,434 ("the '434 patent"); 5,851,899 ("the '899 patent");

6,495,918 ("the '918 patent"); 6,593,240 ("the '240 patent"); 6,714,055 ("the '055 patent"); and 6,103,456 ("the '456 patent"). (A2886-A2892.)

2. At the evidentiary hearing Qimonda only pursued its allegations with regard to the '670, '434, '899, and '918 patents. As relevant to this appeal, with respect to the '899 patent, Qimonda asserted that semiconductor chips manufactured pursuant to LSI's G12, Gflx, and AL12 processes and downstream products containing chips manufactured from those processes infringed claims 1, 2, 7, 22, and 23 of the '899 patent. Qimonda also asserted that the domestic industry requirement was satisfied because Qimonda's 110 nm 256 Mb DDR1 Mobile SDRAM ("256 Mb SDRAM") process practices claim 22 of the '899 patent.

3. The presiding administrative law judge ("ALJ") issued a final initial determination finding that there was no violation of Section 337 with respect to any of the four patents asserted at the hearing.

The ALJ's determination was based on his findings that there was neither infringement nor practice by a domestic industry product with respect to the '899 patent. The ALJ, however, found that the importation and jurisdictional requirements, and economic prong of the domestic industry had been satisfied. (A24, A25, A51, A253-A254.)

The ALJ's determination of no violation with respect to the '899 patent was based entirely upon a construction of independent claim 1 as requiring that the etching step — i.e., "removing at least a portion of the insulating material covering the active regions" (A683 at col. 9:7-8) – to remove *all* the insulating material covering the active regions not covered by the etching mask. The ALJ gave the same construction to a similar claim element in independent claim 22 of the '899 patent; dependent claims 2, 7, and 23 all incorporated the independent claims 1 and 22 limitation.

a. The key element of claim 1 of the '899 patent at issue in this appeal (and thus the similarly worded element of claim 22) recites that the etching step of "removing at least a portion of the insulating material from the action" includes:

> depositing a mask layer over the insulating material;
>
> patterning the mask layer to expose at least a portion of the insulating material over the active regions; and
>
> removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials; and wherein the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions.

Qimonda argued that this "term should be construed to only require removal of a sufficient amount of the insulating material over the active regions, for the purpose of shortening the subsequent chemical-mechanical polishing (CMP) step." *Id.* The ALJ concluded, however, that "claim 1 of the '899 patent teaches that removing at

least a portion of the insulating material covering the active regions refers to *all* of that portion of the active regions that were exposed when the patterned mark was in place." (A150 (emphasis added).)

b. With respect to

c. Finally, with respect to the technical prong of the domestic industry requirement, the ALJ concluded that Qimonda could not show that its 256 Mb SDRAM process practices claim 22 of the '899 patent. Specifically, the ALJ found that Qimonda could not satisfy

4. Qimonda filed a petition for review, *inter alia*, of the ALJ's non-infringement and domestic industry prong findings with respect to the '899 patent. LSI, Seagate, and the ITC's Office of Unfair Import Investigation did not petition the ITC for review of any of the ALJ's findings or conclusions. The ITC issued its final determination in which it determined not to review any portion of the ALJ's initial decision relating to the '899 patent, thereby adopting those portions. This appeal follows.

SUMMARY OF THE ARGUMENT

The ITC's determination of no violation of Section 337 with respect to the '899 patent should be reversed because it turns entirely on an erroneous claim construction.

A. The ITC erred in construing the etching step in claims 1 and 22 of the \`899 patent to require that *all* the exposed portion of the insulating material be removed so that the underlying active regions are exposed.

1. The ALJ's construction of the etching step – adopted in full by the ITC – cannot be reconciled with the claim language. By its very terms, the '899 patent recites that the etching step only "remov[es] *at least a portion* of the insulating material covering the active regions." (A683 at col. 9:7 (emphasis added); *see also* A684 at col. 12:11-12.) The etching step thus does not require that *all* the insulating material be removed; rather, the subsequent planarization step does that by smoothing the chip surface "to expose the active regions." (A683 at col. 9:10.) As such, contrary to the ALJ's requirement that all the exposed insulating material be removed, the claim language "removing the exposed portion of the insulating material over the active regions" – which is nothing more than a definitional element of the etching step – cannot be construed to alter the scope of the etching step to mandate that what it explicitly does not.

2. Nor does the specification teach that all the exposed insulating material covering the active regions be removed in the etching step. The specification states only that the etching step must remove a portion of the excess insulating material so that the amount of time it takes to planarize the substrate surface is reduced, thereby avoiding the problem in the prior art of excess erosion – i.e., dishing – in the STI regions. Thus, the specification teaches that during the etching step "[p]ortions of the insulation layer [are] selectively removed, enabling the subsequent planarization step, which exposes the active regions, to be shortened." (A680 at col. 3:36-59.)

The ALJ, however, reached the opposite conclusion by reading limitations from a preferred embodiment into the claims at issue. The ALJ's construction imports one particular type of etching method – an "oxide selective" technique that removes all the insulating material to expose the active regions not covered by the etching mask – from a preferred embodiment. But the language of claims 1 and 22 do not specify that any particular etching technique must be used. To the contrary, the specification teaches only that a "suitable etching technique" to remove a portion of the insulating material, not that a particular oxide selective method that removes all of it, must be used. This Court has held that "particular embodiments appearing in the written description will not be used to limit claim language that

has broader effect." *Innova/Pure Water, Inc. v. Safari Water Filitration Sys.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004).

3. The prosecution history of the '899 patent further confirms that the ALJ erred in his construction of claims 1 and 22. This history demonstrates that the inventor of the '899 patent intended only that the etching step remove at least a portion of the exposed insulating material covering the active regions – rather than all of the exposed insulating material covering the active regions – in order to shorten the amount of time needed for planarization.

B. Under the proper construction of claims 1 and 22 of the '899 patent – one that requires only a portion of the exposed insulating material covering the active regions to be removed during the etching step – there can be no dispute that LSI and Seagate violated Section 337. The evidence at hearing demonstrated that

Because this ruling turned on the erroneous construction of claim 22, this finding should be set aside.

STANDARD OF REVIEW

Claim construction is a question of law and is reviewed *de novo*. *Kinik v. ITC*, 362 F.3d 1359, 1361 (Fed. Cir. 2004).

Whether an accused product infringes or a domestic product practices correctly construed claims is a question of fact. *Id.* Factual findings are reviewed to ascertain whether they are supported by substantial evidence on the record as a whole. *Id.* Factual findings are supported by substantial evidence if the findings are supported by "such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Id.* (citation and quotation marks omitted).

ARGUMENT

Section 337 of the Tariff Act makes unlawful, *inter alia*, "[t]he importation into the United States, the sale for importation, or the sale within the United States after importation" of "articles" that "infringe a valid and enforceable United States patent" so long as "an industry in the United States, relating to the articles protected by the patent . . . , exists or is in the process of being established." 19 U.S.C. § 1337(a)(1)(B)(i), (a)(2).

The ALJ's initial determination of no violation of Section 337 with respect to the '899 patent, which was adopted in full by the Commission, is based entirely

on the ALJ's construction of the claim language "removing the exposed portion of the insulating material over the active regions" which is a part of the etching step of the chip fabrication process where "at least a portion of the insulating material covering the active regions" is removed before planarization and the active regions are exposed. The ALJ construed this limitation to require that *all* the exposed portion of the insulating material be removed so that the active regions on the substrate are exposed during the etching step. But that construction cannot be reconciled with the patent. Correctly construed, the language "removing the exposed portion of the insulating material over the active regions" requires only the removal of a portion of the insulating material not overlain by photoresist. Because the ALJ's ruling that [redacted] that determination should be reversed.

A. Correctly Construed, "Removing The Exposed Portion Of The Insulating Material Over The Active Regions" Means Only That "At Least A Portion Of The Insulating Material From The Active Region" Must Be Removed

The first step in interpreting a claim term is to examine the claim language itself, because it is "the claims of a patent [which] define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quoting *Innova/Pure Water, Inc. v. Safari Water*

Filtration Systems, Inc., 381 F.3d 1111, 1115 (Fed. Cir. 2004)) (internal quotation marks omitted). The words of the claim are normally given their ordinary and customary meaning, which is "the meaning that term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1312-13. Claims must be construed "in the context of the entire patent, including the specification," *id.* at 1313, which, other than the claim language itself, provides the primary basis for construing the claims, *id.* at 1315 (quoting *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 452 (Fed. Cir. 1985)). Here, the claim language, the specification, and the prosecution history all conclusively establish that the etching step of the manufacturing process requires only a removal of "at least a portion of the insulating material covering the active regions" prior to the planarization of the substrate surface.

1. Claim language

At issue in this appeal are two independent claims – claims 1 and 22 – and three dependent claims – claims 2, 7, and 23. Under the ALJ's construction of the patent, the etching step must remove all the insulating material that is not covered by the etching mask so that the active regions are exposed. But nothing in these claims requires that the etching step ("removing at least a portion of the insulating material covering the active regions" (A683 at col. 9:7-8)) must remove, as construed by the ALJ, *all* "the insulating material from those areas not covered by

the photoresist layer to expose the surface of the semiconductor substrate." (A155; *see also* A151 (explaining that this claim element requires the removal of "*all* of the item being described," which is the exposed portion of the insulating materials).)

a. The plain language of both independent claims (claims 1 and 22) requires the etching step remove only "at least a portion" – not "all" – of the insulating material covering the active regions *prior* to the planarizing step, which removes all remaining insulating material to expose the active regions on the substrate. Claim 1 recites:

> [the etching step as] removing *at least a portion* of the insulating material covering the active regions; and
>
> [the planarizing step as] planarizing the surface of said substrate to expose the active regions.

(A683 at col. 9:7-10:9 (claim 1) (emphasis added); *see also* A684 at col. 12:11-14 (claim 22).) This claim language makes clear that the planarizing step, not the etching step, removes "all" of the remaining substrate "to expose the active regions." Had the inventors of the '899 patent intended for the etching step to remove "all" or the insulating material covering the active regions, the claim

language would not have used the phrase "at least a portion" and would not have required the planarizing step "to expose the active regions."[3]

b. Nor does the definition of "removing at least a portion of the insulating material covering the active regions" in the claim language support the ALJ's narrow construction of requiring all the exposed insulating material to be removed. The claim language defines the etching step to include (1) depositing a layer of photoresist onto the insulating material, (2) patterning the photoresist so

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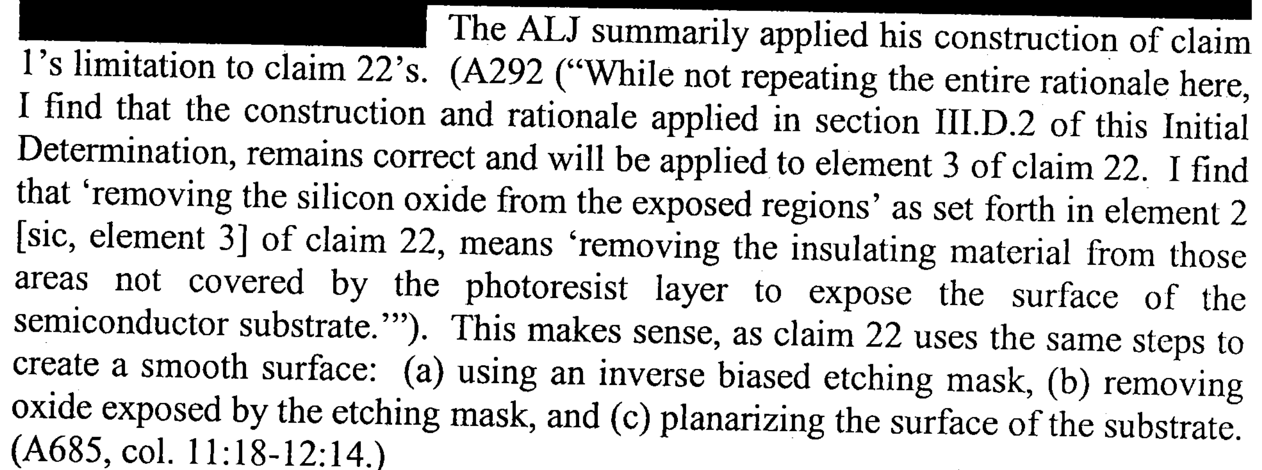
[3] Although claims 1 and 22 differ slightly in the language for their corresponding etching step limitations, the ALJ, the parties, and the Office of Unfair Import Investigation treated them as identical and applied the rationale and construction of claim 1 to claim 22 throughout these proceedings.



The ALJ summarily applied his construction of claim 1's limitation to claim 22's. (A292 ("While not repeating the entire rationale here, I find that the construction and rationale applied in section III.D.2 of this Initial Determination, remains correct and will be applied to element 3 of claim 22. I find that 'removing the silicon oxide from the exposed regions' as set forth in element 2 [sic, element 3] of claim 22, means 'removing the insulating material from those areas not covered by the photoresist layer to expose the surface of the semiconductor substrate.'"). This makes sense, as claim 22 uses the same steps to create a smooth surface: (a) using an inverse biased etching mask, (b) removing oxide exposed by the etching mask, and (c) planarizing the surface of the substrate. (A685, col. 11:18-12:14.)

that the photoresist covers the non-active regions and part of the active regions, and (3) removing a portion of the insulating material not overlain by photoresist:

> wherein removing of at least a portion of the insulating material from the active regions includes:
>
> depositing a mask layer over the insulating material;
>
> patterning the mask layer to expose at least a portion of the insulating material over the active regions; and
>
> removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials.

(A683 at col. 9:12-20 (claim 1); *see also* A684 at col. 12:8-13 (claim 22).)

In construing "removing the exposed portion of the insulating material over the active regions," the ALJ concluded that the use of the definite article "the" before "exposed portion" means that "*all*" of the insulating material over the exposed portion over the active regions must be removed, and he reasoned that his construction was "strengthened by the claim's teaching that unexposed portions of the insulating material are to be left *in situ*." (A151.) In other words, under the ALJ's construction, *all* of the exposed portions of insulating material must be removed down to the active regions on the substrate and *all* of the unexposed portions must remain.

Contrary to the ALJ's reading, however, the plain and ordinary meaning and usage of the article "the" is not "all"; rather, in the context of the claim language

"*the* exposed portion" refers to *where* the etching of the insulating material is to occur.

Likewise, that the claim language requires that the unexposed portion of the insulating material – i.e., the insulating material protected under the photoresist mask – be left intact (A683 at col. 9:18-19 ("leaving unexposed portions of the insulating materials")) does not dictate that it is the only insulating material that can remain after the etching step. Rather, that language explains where etching should *not* occur. *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms.").

The claim language, by using the phrase "removing the exposed portion of the insulating material over the active regions," thus ensures that some etching occurs over the entire exposed portion of the insulating material not covered by the photoresist mask (for that reason the claim language could not say at least a portion of the exposed area, because that would mean that *no* etching might occur on some of the exposed portion of the insulating material). The etching of some amount of the insulating material over the entire portion of the exposed area reduces the amount of time needed for the planarization step. (A680 at col. 3:56-63.) But that does not mean, and indeed does not say, that the etching must be sufficient to completely expose the active areas, which is what the planarization step does.

Indeed, one of ordinary skill in the art reading the claim language would not construe that language to require the removal of all of the exposed insulating material. Rather, he or she would know that the removal of all the exposed insulating material could not be the meaning because it would serve no purpose and would cause reliability problems by requiring the use of a thick silicon nitride layer to protect the underlying substrate. (A2295 at Q&A 87-89.) This is so because, if the etching step must remove all of the exposed insulating layer, it will necessarily remove portions of the underlying silicon nitride layer protecting the substrate. (*Id.*) One of ordinary skill in the art would not read the limitations in claims 1 and 22 to remove all the exposed insulating material because the use of a thick silicon nitride layer introduces reliability issues. (*Id.*)

c. When the claim is read in context with the claim's description of the planarizing step, it becomes even clearer that the ALJ's construction should be rejected.

The claim language expressly recites the planarizing step as exposing the active region by removing any insulating material left after the etching: "planarizing the surface of said substrate *to expose* the active regions." (A683 at col. 10:57-58 (emphasis added).) By contrast, the etching step contains no such requirement that the active regions be exposed, as it is focused only on "removing the exposed portion of the insulating material over the active regions" – those

portions of the insulating material not covered by the photoresist. (A683 at col. 9:18-19.) Under the ALJ's construction, the etching step would necessarily "expose the active regions" prior to the planarizing step, which is something that the '899 patent clearly does not claim.

2. The specification

a. The specification confirms that the '899 patent does not require that *all* the exposed portion of the insulating material over the active regions be removed in the etching step. *Phillips*, 415 F.3d at 1315 (noting that the specification "is the single best guide to the meaning of a disputed term"). The specification repeatedly describes the etching step as removing a sufficient amount of excess insulating material so that the duration of the planarizing step can be shortened. And nowhere does the specification describe the invention as requiring an etching step that removes *all* of the insulating material not covered by the photoresist mask, which is how the ALJ construed the claim language.

As described in the specification, the invention of the '899 patent is a method of etching away a portion of the excess insulating material so that the duration of the subsequent planarizing step can be shortened. (A681 at col. 6:48-50; *see also* A680 at col. 3:36-62; A681 at col. 6:19-20; col. 6:22-30; col. 6:35-36; col. 6:40-45; col. 6:48-50; col. 6:53-59; A682 at col. 7:17-22; col. 8:4-8; col. 8:15-21; col. 8:34-37.) As discussed above, a planarizing step with too long of a

duration results in excess insulating material being removed from the STIs, which in turn results in a non-planar surface. (A679 at col. 2:51-58; pp. 7-9 *supra*.)

The specification thus teaches that the invention avoids the problem of excess erosion of the insulating material by shortening the duration of the planarizing step: "In accordance with the invention, the CMP step is shortened to avoid excessive erosion of the STIs and narrow active regions." (A681 at col. 6:48-50; *see also* A680, at col. 3:59-62; A681 at col. 6:26-30; col. 6:48-50; A682 at col. 8:4-8; col. 8:15-21; col. 8:34-37.) The duration of the planarizing step depends on the amount of insulating material that needs to be removed by the planarizing step. (*Id.* at col. 6:36-42.) Therefore, in order to shorten the planarizing step, the invention of the '899 patent, as described under the "Summary of the Invention," and "Detailed Description of the Invention," uses an etching step in which "[p]ortions of the insulation layer [are] selectively removed, enabling the subsequent planarization step, which exposes the active regions, to be shortened." (A680 at col. 3:56-59.) A further description of the invention makes it clear that the invention only requires that enough of the insulating material, rather than all of that material, be removed prior to the planarizing step so that the excess erosion problem is avoided:

> *In accordance with the invention,* the CMP step is shortened to avoid excessive erosion of the STIs and narrow active regions. In one embodiment, shortening of the CMP step is achieved by selectively removing

> portions of the oxide from the triangular-shaped oxide regions above the active areas. By reducing the amount of oxide needed to be removed in order to expose the active areas, the corresponding CMP step is shortened. *Typically, the amount of oxide that is removed from the active regions is sufficient to effectively shorten the CMP step so as to expose the active areas without excessive oxide erosion occurring in the STIs, thus resulting in a substantially planar surface.*

A681 at col. 6:48-59 (emphasis added).)

Moreover, the specification also does not describe the etching step as exposing the active regions on the substrate (as the ALJ's construction would require), which would occur if the etching step removed all of the insulating material not overlain by photoresist. Rather, the specification teaches that the active regions are exposed by the planarization step, which occurs after the etching step: "Portions of the insulation layer is selectively removed, enabling the subsequent planarization step, which exposes the active regions, to be shortened." (A680 at col. 3:56-59 (emphasis added); *see also* A681, at col. 6:19-20; col. 6:22-25; col. 6:35-36; col. 6:40-45; col. 6:53-59; A682 at col. 7:17-22.)

b. Notwithstanding the broad claim language and the above discussed teachings of the specification, the ALJ found support for his more narrow interpretation of the etching step by reading in limitations from a preferred embodiment into the claims at issue. (A152-A154.) This is a basic error of claim construction, as this Court has held that "particular embodiments appearing in the

written description will not be used to limit claim language that has broader effect." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004); *see also Liebel-Flarshem Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed Cir. 2004) ("Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using "words or expressions of manifest exclusion or restriction.") (internal quotation marks and citation omitted).

Under the ALJ's construction in the initial determination, it is clear that a preferred embodiment using a particular etching method, reactive ion etching ("RIE"), is imported into the claims:

> The Detailed Description of the Invention makes clear that the invention's purpose is achieved by using, for example, an RIE, which is described as "oxide selective." Because the RIE etching step is oxide selective, the silicon substrate and resist act as etch stops. Thus, the specification says, "the RIE removes only the HDP-CVD oxide layer 52, exposing the semiconductor substrate above those areas not covered by the photoresist layer 60." (JX-8 at 7:47-52.)

(A152.) But, contrary to the ALJ's statement, the specification's discussion of RIE plainly refers to Figures 4A to 4D, which the ALJ even acknowledges is only "a preferred embodiment of the inventive method," not the invention more generally. (A680 at col. 4:18-21; A162 ("In the description of the preferred embodiment, the

'899 patent uses Figures 4A through 4D, inclusive to describe the process used . . . .")).) It is this preferred embodiment that uses a RIE etching step, a particular oxide selective etching method which exposes the semiconductor substrate not covered by the etching mark. And the ALJ's decision to import the RIE etching, or any other oxide selective etching method, into the invention generally cannot be reconciled with the broader claim language.

This is confirmed by the plain language of claim 1, which does not require that the etching be performed by RIE or any other particular etching method (oxide selective or otherwise). Indeed, the specification identifies RIE as an example of one etching methods: "The regions of the oxide layer 52 unprotected by photoresist are then etched using a suitable etching technique *(such as* RIE)." (A682 at col. 7:44-46 (emphasis added). Thus, it was improper for the ALJ to use the preferred embodiment using the RIE etching method to limit the scope of the claim language.

3. *Prosecution history*

Although not necessary to show the ALJ's claim construction error, the prosecution history further confirms that claims 1 and 22 do not require that all the exposed portion of the insulating material be removed to expose the active regions on the substrate during the etching step. *Phillips*, 415 F.3d at 1317 (explaining that the prosecution history is a valuable tool for claim interpretation "inform[ing] the

meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be"). The patentee's statements during prosecution confirm that he intended, and the patent examiner understood, that the claim language at issue should be given its ordinary and customary meaning and that he in no way disavowed any portion of that meaning by limiting the invention to the preferred embodiment.

After the patent examiner rejected application claim 1, the applicant amended the claim to add the claim language at issue. (A799-A813, '899 patent Pros. Hist., Response to Office Action (Nov. 18, 1997) at A800.) In the statement that accompanied the amendment, the applicant explained that the added language – "removing at least a portion of the insulating material covering the active regions" – meant that the etching step would remove enough of the excess insulating material so that the planarization step would be short enough to create a planar surface:

> In contrast, claim 1 recites 'removing at least a portion of the insulating material covering the active regions' before planarization. *As discussed, the removal of at least a portion of the insulating material shortens the amount of time required for planarization, which results in reduced erosion or dishing of the insulating material in the isolation regions.* The removal of at least a portion of insulating material covering the active regions before planarization is nowhere taught or suggested in [the prior

art]. As such, the Applicant respectfully requests withdrawal of the rejection based on [the prior art].

(A811 (emphasis added); *see also* A809-A810 ("In one embodiment of the invention, at least a portion of the material above the active regions is removed. By removing at least a portion of the material above the active regions, the polish time is reduced, thereby avoiding excessive erosion or dishing of the isolation material in the isolation regions. As a result, a more planar surface is produced.").

Thus, the prosecution history makes clear that, contrary to the ALJ's construction, the patentee did not limit the claim language during prosecution to require that *all* of the insulating material not overlain by photoresist be removed by etching, by the use of the RIE etching or some other oxide selective method. Rather, the patentee's explanation of the claim language disputed in this case demonstrates that the phrase should be construed as requiring that the etching only needs to remove some of the insulating material not overlain by photoresist to reduce the amount of time needed for planarization.

B. Under The Correct Claim Construction, The Undisputed Facts Demonstrate That The Commission's Determination Of No Violation With Respect To The '899 Patent Should Be Reversed

1. Infringement

Under the proper construction of "removing the exposed portion of the insulating material over the active regions" as requiring that the etching step remove only some of the exposed insulating material not covered by the etching

mask, there is no dispute that LSI and Seagate violated Section 337 with respect to the ’899 patent.

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REDACTED

[REDACTED] *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 988 (Fed. Cir. 1999) ("Because the relevant aspects of the accused device's structure and operation are undisputed in this case, the question of whether Zebco's AutoGuide product infringes the claims of Johnson's '835 patent turns on the interpretation of those claims."); *K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1362 (Fed. Cir. 1999); *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1578 (Fed. Cir. 1996).

2. Domestic industry requirement

The ALJ's conclusion that Qimonda's 256 Mb DRAM chip process at Qimonda's Richmond, Virginia manufacturing facility did not practice claim 22 also turns entirely on the erroneous claim construction of "removing the exposed portion of the insulating material over the active regions." The ALJ noted that "Qimonda has argued consistently that construction of the term requires removal of a sufficient amount of the insulating material over the active regions, for the purpose of shortening the subsequent chemical-mechanical polishing (CMP) step." (A292.) [REDACTED]

[REDACTED]

[REDACTED] *Johnson Worldwide Assocs.*, 175 F.3d at 988; *K-2 Corp.* 191 F.3d 1356 at 1362; *Athletic Alternatives,* 73 F.3d at 1578.

CONCLUSION

The Commission's determination that Seagate and LSI did not violate Section 337 of the Tariff Act should be reversed.

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Respectfully Submitted,

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