[; CX-0567C ; CX-0568C ; CX-0569C ; CX-0570C 1; CX-1596C .]

iii. Realtek – Analysis Under Alternate Construction

Realtek's chips include [ ][64]. CX-1596C (Negus WS) at Q&A 315. This structure is described by the module [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000620-22, 25-27,647-48,2190,92,93,95,2195-96,2410,11,13,18-20; CX-1596C (Negus WS) at 98. [

] CX-1596C (Negus WS) at Q&A 316; CX-0298C (Realtek Source Code) at REA837ITC-SC-00002190,92,93,95 [ ]; REA837ITC-SC-00002195-96 [ ]; REAT837ITC-SC-00002410,11,13,18,19 [ ]; REA837ITC-SC-00002413,19-20 [ ]; REA837ITC-SC-00000620-22, 26 [ ]; REA837ITC-SC-00002413,19,20 [ ].

[

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000626,647,2196,2419; CX-1596C (Negus WS) at Q&A 317. Exemplary datasheets for Realtek's chips indicate the presence of [ ] *See, e.g.*, CX-0572C [ ]) at 123-24; CX-0579C [ ]) at 107-108; CX-0580C [ ]) at 49-51; CX-0581C [ ])

at 34; CX-0582C [ ]) at 33; CX-0583C [ ]) at 32; CX-1596C (Negus WS) at Q&A 318.

iv. Funai – Analysis Under Alternate Construction

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips or Realtek's chips, the same evidence described above shows that this limitation is met by structure within Ralink's chips or Realtek's chips and is met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 319.

v. Doctrine of Equivalents

In addition to arguing literal infringement of this claim limitation under Complainants' proposed construction, Complainants also allege that the accused products satisfy this claim limitation under the doctrine of equivalents in the event Respondents' proposed construction is adopted. *See* Compls. Br. at 464-66. Complainants' doctrine of equivalents argument is not persuasive, however, because there is no evidence that the differences between the claimed and accused "receiver counter" are insubstantial.

Complainants argue that the function of the claimed "receiver counter" is "to provide a local timer within the 'receiver.'" Compls. Br. at 466. The '867 specification, however, states: "[E]nergization of the receiver 48 is controlled by a modulo n counter 58 which functions as a timer to wake up the station 12.1 from a doze state to receive the TIM packet 28 transmitted from the access point 14." JX-0005 ('867 patent) at col. 6, lns. 3-6. "[T]he receiver counter tells the receiver to wake up by approaching the value 'n,' because TIM generation signals are generated 'each time the modulo n counter 22 in the access point 14 reaches its value n.'" *Id.* at col. 7, lns. 1-6. During prosecution, the applicants described the function the same way . *See, e.g.*, JX-0006 (file history of '867 patent) at JX-0006.0232-34; RX-1165 (prosecution history of

'661 application) at REA837ITC00000498-500. Accordingly, the function of the claimed receiver counter is to "wake up" to receiver. Complainants have not shown that the alleged receiver counters in the accused products perform this function.

c. a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp field,

i. 802.11

Respondents' products are [ ] CX-1596C (Negus WS) at Q&A 326. [ ] Respondents' products are [ ] *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §11.1.1.1; CX-1596C (Negus WS) at Q&A 326-33. Such an AP is the "transmitter" of this claim element. *See, e.g.*, JX-0005 ('867 patent) at Figs. 1, 2; col. 2, lns. 48-62; col. 4, lns. 52-53; CX-1596C (Negus WS) at Q&A 326-33. The AP (or "transmitter") is required to "periodically transmit special frames called Beacon frames that contain a copy of its TSF timer to synchronize the TSF timers of other STAs in a BSS." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §11.1.1.1; CX-1596C (Negus WS) at Q&A 326-33. Receivers must be capable of receiving these Beacon frames "at a nominal rate." CX-1596C (Negus WS) at Q&A 326-33. Each STA (or "receiver") "shall always accept the timing information in Beacon frames sent from the AP servicing its BSS." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §11.1.1.1; CX-1596C (Negus WS) at Q&A 326-33. The interval between Beacon frames is defined by the dot11BeaconPeriod parameter of the STA." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §11.1.2; CX-1596C (Negus WS) at Q&A

[55] "AP" is an acronym for "access point."

326-33. Respondents' products are therefore [

] *Id.*

Further, any 802.11 STA device that interoperates with any of the 802.11 radio-based PHY layers must have at least a "modulator" and a "demodulator," and hence a "radio modem." CX-1596C (Negus WS) at Q&A 331.

Finally, the "Beacon frames" sent by an 802.11 AP always include at least a "Timestamp field." *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at §§7.2.3.1, 7.3.1.10, 11.1.2, Table 7-8; CX-1596C (Negus WS) at Q&A 333. "Beacon frames" that are sent "periodically" by an 802.11 AP disclose the "transmission signal from a transmitter" of this claim element and therefore any 802.11 standard STA device with a compatible TSF timer implementation must comprise structure that meets the limitations of this claim element. *Id.*

ii. Ralink

[

CX-0561C

; CX-1596C

CX-0561C

; CX-1596C

]"

[

.]

[

JX-0014C

CX-0562C ; CX-0563C ; CX-0564C

; CX-0565C ; CX-0566C

; CX-0567C ; CX-0568C

; CX-0569C ; CX-0570C ;

CX-1596C .]

[

.]

iii. Realtek

Realtek's chips, [ ] comprise a structure described by the module

[

] *See, e.g.*, CX-0298C (Realtek Source Code) at

REA837ITC-SC-000002582,2616,2633,2637-38,2792-93,3026-27; CX-1596C (Negus WS) at

Q&A 339. [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-000002637-38, 2792-93, 3026-27; CX-1596C (Negus WS) at Q&A 340. [

] *Id.* [

] *Id.*

Moreover, testimony from Realtek's fact witness [ ] indicates that Realtek's chips include this capability. *See* JX-0017C [ ] at 40. Datasheets for Realtek's chips illustrate [

] *See, e.g.*, CX-0571C [ ]) at 8; CX-0572C [ ]) at 11, 23-24; CX-0573C [ ]) at 8; CX-0575C [ ]) at 8; CX-0576C [ ]) at 9; CX-0577C [ ]) at 9; CX-0578C [ ]) at 10; CX-0579C [ ]) at 107-08, 116; CX-0580C [ ]) at 49-51, 57; CX-0581C [ ]) at 34, 41; CX-0582C [ ]) at 33, 37; CX-0583C [ ]) at 32, 38; CX-0584C [ ]) at 9-10; CX-0585C [ ]) at 10; CX-1596C (Negus WS) at Q&A 342.

Realtek's chips need not contain [ ] to meet this claim limitation. CX-1596C (Negus WS) at Q&A 343. Even if certain Realtek chips did not comprise [ ] any [ ] would still meet the limitation of this claim

element since each such chip is intended for use [ ] and must have at least [ ] *Id.*

iv. Funai

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips. This limitation is also met by structure within Funai's products. CX-1596C (Negus WS) Q&A 344; *see* CX-0587C (Funai Source Code) at FUNAI-ITC837-SC-00000068.

d. the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer,

Applying the claim construction adopted above, the accused products do not satisfy the claim limitation "a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer." This limitation is construed to mean "a timestamp representing a value m within the range 0 to n in the counter of the transmitter, where n represents the interval between transmission signals."

Complainants concede there is no literal infringement under the adopted construction. *See* CX-1596C (Negus WS) at Q&A 354; Negus Tr. 407-409. The accused timestamp is not the length of delay, or "value m," and is not within a cyclical count from 0 to the timer interval, or "n." RX-2811C (Vojcic WS) at &QA 232-33; RX-2813C (Heegard RWS) at Q&A 367-68. Rather, [ ] *Id.* This is consistent with the IEEE 802.11 standard, which requires 64-bit

counters in the access points and stations and a corresponding 64-bit timestamp field. *Id.*; RX-0013C (IEEE Std. 802.11-2007) at 837RALINK000001482.

If, however, Complainants' proposed construction of "a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer" were adopted such that the term meant "a timestamp representing a value of a counter in the transmitter," then the evidence shows that the accused products would satisfy this claim limitation. The following analysis sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. Analysis Under Alternate Construction

As described above, in an 802.11 WLAN the AP periodically transmits Beacon frames that include timestamp fields. The timestamp field is a copy of the AP's TSF timer, which is a transmitter timer with a maximum value of 2^{64} microseconds. The "timestamp field" is thus a value m in the transmitter timer's count sequence between 0 and 2^{64}. CX-1596C (Negus WS) at Q&A 351.

ii. Doctrine of Equivalents

In addition to arguing literal infringement of this claim limitation under Complainants' proposed construction, Complainants also allege that the accused products satisfy this claim limitation under the doctrine of equivalents in the event Respondents' proposed construction is adopted. *See* Compls. Br. at 471-73. Complainants' doctrine of equivalents argument is not persuasive, however, because there are substantial differences between the claimed and accused timestamp in the accused products. RX-2811C (Vojcic WS) at Q&A 234-39. Unlike the claimed timestamp, the accused timestamp [

] *Id.*

The function of the claimed timestamp is to inform the receiver of the length of the delay. JX-0005 ('867 patent) at col. 7, lns. 1-21; RX-1165 (file history of '661 application) at REA837ITC00000526. The applicants told the USPTO that the claimed timestamp has the "very beneficial characteristics of providing information to the receiver as to whether . . . there was a delay . . . and how long was that delay." RX-1165 (file history of '661 application) at 109, n.*****. Thus, with the claimed timestamp, a receiver has a reference point to know the time of the next scheduled transmission. RX-2811C (Vojcic WS) at Q&A 235-38.

The accused timestamp [

]

RX-2811C (Vojcic WS) at Q&A 235. [

] *Id.*

The way the claimed timestamp performs its function is by representing the amount of delay and resetting the receiver counter to start counting at the "m counts" of delay. JX-0005 ('867 patent) at col. 7, lns. 1-21; RX-1165 (file history of '661 application) at REA837ITC00000526; RX-2811C (Vojcic WS) at Q&A 236. The accused timestamp [

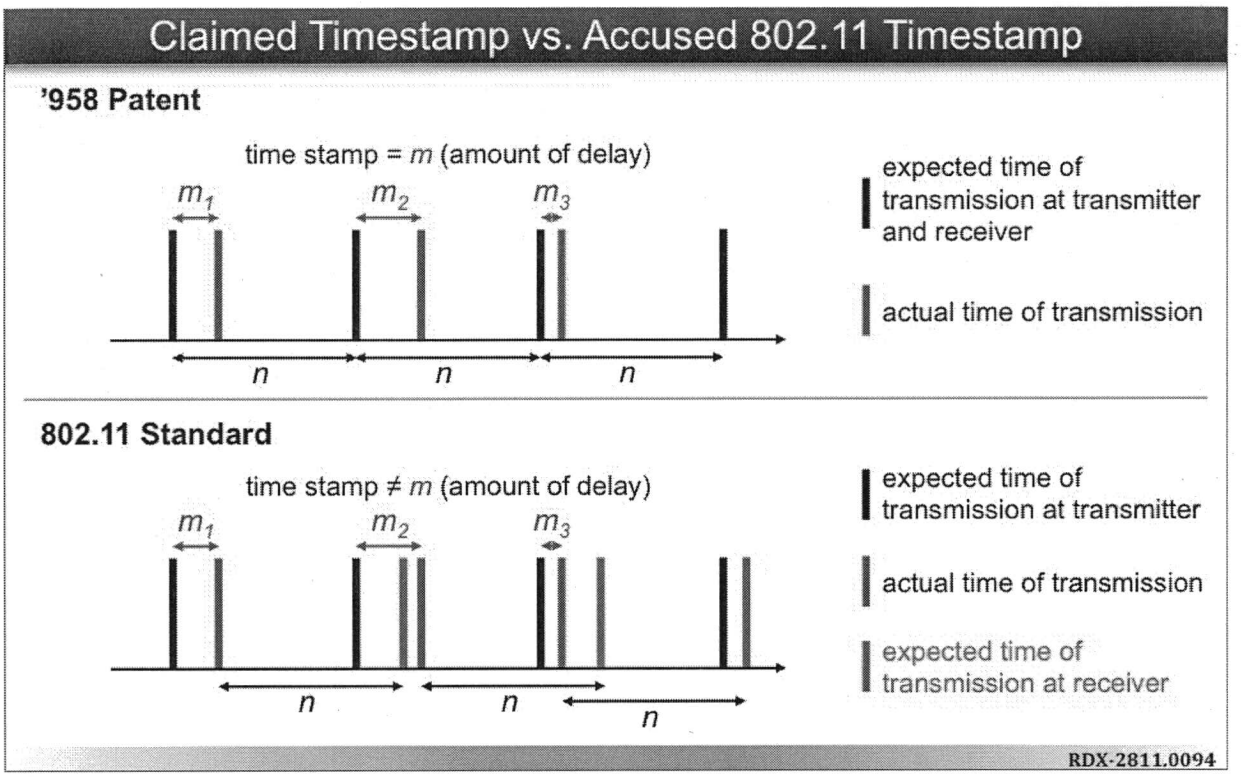
]

RX-2811C (Vojcic WS) at Q&A 236.

The result of using the claimed timestamp is that the receiver receives information about the length of the delay for knowing when the next frame is scheduled to arrive. JX-0005 ('867 patent) at col. 7, lns. 16-19; RX-1165 (file history of '661 application) at REA837ITC00000526;

RX-2811C (Vojcic WS) at Q&A 237-39. [

] The illustration below shows the substantially different result. RDX-2811.0094; RX-2811C (Vojcic WS) at Q&A 237-39.



The top portion of the illustration above shows the result of using the claimed timestamp. RX-2811C (Vojcic WS) at Q&A 238; RDX-2811.0094. The three blue lines show the actual time of transmission, and indicate three different amounts of delay, m_1, m_2, and m_3. *Id.* Inasmuch as the claimed timestamp is equal to the amount of delay m, the receiver counter can begin counting from m, and will arrive at the timer interval n, at the same time as the transmitter counter. *Id.* As a result, the expected time of transmission at the receiver is the same as the expected time of transmission at the transmitter, as the black lines show. The patent explains the importance of this result:

> [Since] the counter in the station 12.1 is accurately synchronized with the counter 22, the station 12.1 can be controlled to accurately wake up in time to receive only every xth TIM packet without requiring the station 12.1 to wake up unnecessarily early as would be required to assure receipt of the TIM packet if accurate synchronization between the counters 22, 58 was not available. The reduction in the need for early wake up of the station 12.1 advantageously reduces the power consumption of the station 12.1.

JX-0005 ('867 patent) at col. 6, lns. 49-55.

The bottom portion of the above illustration shows the result of using the accused timestamp, [ ] RX-2811C (Vojcic WS) at Q&A 238; RDX-2811.0094. [

] *Id.* [

] RX-2811C (Vojcic WS) at Q&A 238. Without the claimed timestamp, the accused receivers [

]" which the patent teaches against, in order to receive the Beacon frame, with the result that they consume more power. *Id.*; JX-0005 ('867 patent) at col. 6, lns. 49-55.

The claimed and accused timestamps are also not interchangeable. RX-2811C (Vojcic WS) at Q&A 239. The claimed receiver would not work if it received the accused timestamp because the accused timestamp [ ] *Id.* Any attempt to use the arbitrary number from 0 to 2^{64}-1 as a delay would not work because the claimed receiver requires the length of the delay, m, in a count sequence between 0 and the timer interval, n. *Id.*

e. and wherein the timestamp accounts for delays due to a busy signal on a medium access protocol.

Applying the claim construction adopted above, the accused products do not satisfy the claim limitation "the timestamp accounts for delays due to a busy signal on a medium access protocol." The claim terms "accounts for delay," "accounts for delays," and "accounts for a delay" are construed to mean "indicates the amount of delay."

The accused products do not satisfy this claim limitation, because the accused timestamp [ ] RX-2811C (Vojcic WS) at Q&A 253-54. As discussed above, that timestamp is merely [ ] *Id.*

Complainants' expert Dr. Negus concedes there is no literal infringement of this claim limitation under Respondents' proposed construction with respect to claim 20. *See* CX-1596C (Negus WS) Q&A 370, Q&A 451, Q&A 456. There is no literal infringement of any of these claims and no infringement under the doctrine of equivalents for claim 20 (or any other claims) for the same reasons stated above with respect to the "timestamp" phrases. The claimed timestamp that "accounts for delays" informs the receiver of the precise amount of delay due to a busy signal at the transmitter, while the accused timestamp [ ] The claimed timestamp results in accurate synchronization, whereas the accused timestamp does not.

If, however, Complainants' proposed construction of "accounts for delays" were adopted such that the term meant "accounts for the delay in transmission of a signal," then the evidence shows that the accused products would satisfy this claim limitation. The following analysis sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. Analysis Under Alternate Construction

For an 802.11 AP, the transmission of "Beacon frames" must consider that "Though the transmission of a Beacon frame may be delayed because of CSMA deferrals, subsequent Beacon frames shall be scheduled at the undelayed nominal beacon interval" and that each "Beacon frame" is a "transmission according to the medium access rules specified in Clause 9." CX-1596C (Negus WS) at Q&A 359; CX-0116C (802.11 Standard, Jun. 2007) at §11.1.2.1, Fig. 11-1. Clause 9 shows "Physical and virtual carrier-sense functions are used to determine the state of the medium. When either function indicates a busy medium, the medium shall be considered busy; otherwise, it shall be considered idle." *See* CX-0116C (802.11 Standard, Jun. 2007) at §9.2.1; CX-1596C (Negus WS) at Q&A 359.

The transmission signals (or "Beacon frames") that carry the "timestamp" to Respondents' products are not always transmitted exactly when the periodic beacons are scheduled. CX-1596C (Negus WS) at Q&A 361. If there is a busy signal condition on the shared wireless medium, the transmission signals will be delayed. *Id.* at Q&A 362. The 802.11 Standard requires that "a Beacon frame shall set the value of the Beacon frame's timestamp so that it equals the value of the STA's TSF timer at the time that the data symbol containing the first bit of the timestamp is transmitted to the PHY." *Id.* In other terms, the timestamp is set for the actual time the timestamp is transmitted, rather than the scheduled time of transmission. *Id.* This accounts for "delays due to a busy signal on a medium access protocol" by ensuring that the timestamp represents the value of the transmitter TSF timer at the time of transmission. *Id.* If the timestamp were set for the time the transmission signal was scheduled for transmission, the timestamp would not enable accurate synchronization if it were transmitted at a later time due to some delay. *Id.*

ii. Doctrine of Equivalents

In addition to arguing literal infringement of this claim limitation under Complainants' proposed construction, Complainants also allege that the accused products satisfy this claim limitation under the doctrine of equivalents in the event Respondents' proposed construction is adopted. *See* Compls. Br. at 475-77. There is no infringement under the doctrine of equivalents for for the same reasons stated above with respect to the "timestamp" phrases.

4. Claim 23

The record evidence shows that the accused products do not satisfy all limitations of claim 23.

a. The receiver of claim 20,

As shown above, the accused products do not satisfy all limitations of asserted claim 20 under the adopted claim constructions.

b. wherein the transmission signal further includes a header field, which is transmitted before the timestamp field and the traffic pending field.

If Complainants' proposed claim constructions were adopted, the evidence shows that the accused products would satisfy the additional limitation of claim 23.

The 802.11 Standard mandates that the "Beacon frames" received by Respondents' products include a "MAC header" (or "header field") which precedes in time the "Timestamp" field of the "Beacon frame" and the "TIM" field. *See* CX-0116C (802.11 Standard, Jun. 2007) at §§ 7.2.3, 7.2.3.1, Figure 7-18, Table 7-8; CX-1596C (Negus WS) at Q&A 372. In the 802.11 Standard, "TIM" is an acronym for "traffic indication map." CX-0116C (802.11 Standard, Jun. 2007) at § 4. The Standard further provides that "Each bit in the [TIM] corresponds to traffic buffered for a specific STA within the BSS that the AP is prepared to deliver at the time the

beacon frame is transmitted." CX-0116C (802.11 Standard, Jun. 2007) at § 7.3.2.6. Thus, the "TIM" field indicates if there is "traffic pending" for any particular STA and as such is the "traffic pending field" that "indicates for which stations data packets are buffered." CX-1596C (Negus WS) at 121.

5. Claim 24

The record evidence shows that the accused products do not satisfy all limitations of claim 24.

a. The receiver of claim 23,

As shown above, the accused products do not satisfy all limitations of asserted claim 23 under the adopted claim constructions.

b. wherein the header field includes type data indicating a type of the transmission signal.

If Complainants' proposed claim constructions were adopted, the evidence shows that the accused products would satisfy the additional limitation of claim 24.

The 802.11 Standard mandates that the "Beacon frames" received by Respondents' products include "Type" and "Subtype" fields (or "type data") that indicate that the frame is a "Beacon frame." CX-0116C (802.11 Standard, Jun. 2007) at §§ 7.1.3.1, 7.1.2.1.2, 7.2.3, 7.2.3.1, Table 7-1.

6. Claim 26

Independent claim 26 recites every element of claim 20 except "and wherein the timestamp accounts for delays due to a busy signal on a medium access protocol," and adds the limitation "circuitry for adjusting a value, based on the timestamp, at which a count sequence begins at the receiver timer, wherein the receiver counter commences a synchronizing count sequence beginning at the adjusted value." As shown above, the accused products do not satisfy

all limitations of claim 20 under the adopted claim constructions, and therefore do not satisfy all limitations of claim 26. The record evidence does show, however, that the accused products satisfy the additional limitation of claim 26, "circuitry for adjusting a value, based on the timestamp, at which a count sequence begins at the receiver timer, wherein the receiver counter commences a synchronizing count sequence beginning at the adjusted value."

i. 802.11

The 802.11 Standard requires that for Respondents' products the received "timestamp value shall be adjusted by adding an amount equal to the receiving STA's delay through its local PHY components plus the time since the first bit of the timestamp was received at the MAC/PHY interface." CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.4; CX-1596C (Negus WS) at Q&A 384. After circuitry within a STA performs the step of adjusting the received timestamp value, the 802.11 standard further mandates that "the STA's TSF timer shall then be set to the adjusted value of the timestamp." CX-1596C (Negus WS) at Q&A 385; CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.4.

ii. Ralink

[

., CX-0561C (Ralink Source Code) at 837RALINK_SC0000023-25,34-36,43; CX-1596C

CX-0561C ; CX-1596C

]

iii. Realtek

Realtek's [ ] chips comprise a structure described by the module [

] CX-1596C (Negus WS) at Q&A 389.

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002195-96; CX-1596C (Negus WS) at Q&A 389. [ ] chips further comprise a structure described by the module [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002195-96; CX-1596C (Negus WS) at Q&A 389.

Realtek's [ ] chips comprise a structure described by the module [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002418-19; CX-1596C (Negus WS) at Q&A 390. [ ] chips further comprise a structure described by the module [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002418-19; CX-1596C (Negus WS) at Q&A 390.

Realtek's [ ] chips comprise structures described by the modules [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000606-8; CX-1596C (Negus WS) at Q&A 391. [ ] chips further comprise a structure described by the modules [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000606-8; CX-1596C (Negus WS) at Q&A 391.

iv. Funai

For those of Funai's products that interoperate with 802.11 standards devices and contain at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips, and is inherently met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 392.

7. Claim 27

The record evidence shows that the accused products do not satisfy all limitations of claim 27.

a. The receiver of claim 26, further comprising:

As shown above, the accused products do not satisfy all limitations of asserted claim 26 under the adopted claim constructions.

b. circuitry for commencing the synchronizing count sequence after the transmission signal is completely received.

If Complainants' proposed claim constructions were adopted, the evidence shows that the accused products would satisfy the additional limitation of claim 27.

i. 802.11

The 802.11 Standard mandates that "All STAs shall be able to validate every received frame using the frame check sequence (FCS) and to interpret certain fields from the MAC headers of all frames." CX-0116C (802.11 Standard, Jun. 2007) at §§ 7, 7.1. The "FCS" is transmitted last in time for any "Beacon frame" and, therefore, this mandated behavior for Respondents' products requires that a "Beacon frame" (or "transmission signal") be "completely received" prior to synchronization because only complete reception can enable an FCS validation. Without such validation, STAs cannot reliably determine if a particular transmission is a "Beacon frame" or what the contents of fields within the "Beacon frame" are comprised of. *See* CX-0116C (802.11 Standard, Jun. 2007) at §§ 7.2.3, 7.2.3.1; CX-1596C (Negus WS) at Q&A 394. Circuitry for commencing the synchronizing count sequence after the transmission signal is completely received is also explicitly required in the 802.11 Standard by the text "Upon receiving a Beacon frame with a valid FCS and BSSID or SSID, as described in 11.1.2.3, a STA shall update its TSF timer." CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.4; CX-1596C (Negus WS) at Q&A 395.

ii. Ralink

[

CX-1596C

CX-0561C

JX-0014C ; CX-1596C .]

iii. Realtek

Realtek's chips, [ ] comprise a structure described by the module [ ] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002613-16,2763-67,2997-3000; CX-1596C (Negus WS) at Q&A 398. [ ] CX-1596C (Negus WS) at Q&A 399. Realtek's chips further comprise structure [ ] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002613-16, REA837ITC-SC-00002569,75-76, REA837ITC-SC-00002997-3000, REA837ITC-SC-00002944-45,51; CX-1596C (Negus WS) at Q&A 399. [ ] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00002190-96, REA837ITC-SC-00002410-20, REA837ITC-SC-00000620-27, REA837ITC00025078; CX-1596C (Negus WS) at Q&A 399.

iv. Funai

For those of Funai's products that interoperate with 802.11 standards devices and contain at least one of Ralink's chips or Realtek's chips, this limitation is met by structure within Ralink's chips or Realtek's chips and inherently is met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 400.

8. Claim 28

The record evidence shows that the accused products do not satisfy all limitations of claim 28.

a. The receiver of claim 27,

As shown above, the accused products do not satisfy all limitations of asserted claim 27 under the adopted claim constructions.

b. further comprising circuitry for commencing the synchronizing count sequence after a CRC data in the received transmission signal is checked.

If Complainants' proposed claim constructions were adopted, the evidence shows that the accused products would satisfy the additional limitation of claim 28.

"CRC data check" and "FCS" in 802.11 are interchangeable. *See, e.g.*, CX-0116C (802.11 Standard, Jun. 2007) at § 7.1.3.7; CX-1596C (Negus WS) at Q&A 401. Accordingly, the evidence described above relating to dependent claim 27 applies equally to the limitation described in claim 28.

9. Claim 29

The record evidence shows that the accused products do not satisfy all limitations of claim 29.

a. The receiver of claim 26,

As shown above, the accused products do not satisfy all limitations of asserted claim 26 under the adopted claim constructions.

b. further comprising an adder for adding a compensation factor to the value at which the count sequence begins.

If Complainants' proposed claim constructions were adopted, the evidence shows that the Ralink products would satisfy the additional limitation of claim 29.

i. 802.11

The 802.11 standard specifically requires that the "received timestamp value shall be adjusted by adding an amount." CX-1596C (Negus WS) at Q&A 402. This added "amount" is a "compensation factor" and the 802.11 requirement for "adding" indicates that the circuitry for adjusting the timestamp may comprise at least one "adder." *Id.*

ii. Ralink

[

CX-0561C ; CX-1596C

]

iii. Realtek

Complainants argue that Realtek's chips comprise [

] *See,*

e.g., CX-0298C (Realtek Source Code) at REA837ITCSC-00000620-27, 2195-96, 2418-20; CX-1596C (Negus WS) at Q&A 404.

The record evidence shows, however, that the accused Realtek products [

] RX-2811C (Vojcic WS) at Q&A 271-73. The Realtek products [

] *Id.* [

] *Id.*

iv. Funai

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips, this limitation is met by structure within Ralink's chips, and this limitation is met inherently by structure within Funai's products. CX-1596C (Negus WS) at Q&A 405. Inasmuch as Realtek's chips do not satisfy the "adder" limitation, the Funai products incorporating Realtek's chips also do not satisfy this limitation.

10. Claim 30

The record evidence shows that the accused products do not satisfy all limitations of claim 30.

a. The receiver of claim 29,

As shown above, the accused products do not satisfy all limitations of asserted claim 29 under the adopted claim constructions.

b. wherein the compensation factor compensates for propagation delay at the receiver.

If Complainants' proposed claim constructions were adopted, the evidence shows that the accused products would satisfy the additional limitation of claim 30.

i. 802.11

The 802.11 Standard specifically requires that the "received timestamp value shall be adjusted by adding an amount equal to the receiving STA's delay through its local PHY components plus the time since the first bit of the timestamp was received at the MAC/PHY interface." CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.4; CX-1596C (Negus WS) at Q&A 406. This "amount equal to the receiving STA's delay" is a reference to a "compensation factor" that "compensates for propagation delay at the receiver." CX-1596C (Negus WS) at Q&A 406.

ii. Realtek

Realtek's chips comprise [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000620-27,2195-96,2418-20; CX-1596C (Negus WS) at Q&A 408.

iii. Funai

For those of Funai's products that interoperate with 802.11 standards devices and contain at least one of Realtek's chips, this limitation is met by structure within Realtek's chips and

inherently is met by structure within such Funai products. CX-1596C (Negus WS) at Q&A 409.[56]

11. Claim 31

The record evidence shows that the accused products do not satisfy all limitations of claim 31.

a. The receiver of claim 29,

As shown above, the accused products do not satisfy all limitations of asserted claim 29 under the adopted claim constructions.

b. wherein the compensation factor allows for time taken to process the transmission signal at the receiver.

If Complainants' proposed claim constructions were adopted, the evidence shows that the Ralink products would satisfy the additional limitation of claim 31.

i. 802.11

The 802.11 standard specifically requires that the "received timestamp value shall be adjusted by adding an amount equal to the receiving STA's delay through its local PHY components plus the time since the first bit of the timestamp was received at the MAC/PHY interface." CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.4; CX-1596C (Negus WS) at Q&A 410.

ii. Ralink

[

[56] It has not been shown that Ralink chips, or the Funai products that incorporate Ralink chips, satisfy this claim limitation. *See* Compls. Br. at 495.

CX-0561C

; CX-1596C

JX-0014C

.]

iii. Realtek

Complainants argue that Realtek's chips comprise [

] *See, e.g.*, CX-0298C (Realtek Source Code) at REA837ITC-SC-00000620-27,2195-96,2418-20; CX-1596C (Negus WS) at Q&A 413.

The record evidence, however, shows that Realtek's chips do not satisfy this claim limitation. The '867 specification describes two ways to update the receiver counter. JX-0005 ('867 patent) at col. 6, lns. 7-32. In the first method, the timestamp is buffered in a counter register until the TIM packet is processed completely, and in the second method a "processing compensation factor" is loaded directly into the receiver counter so that an intermediate counter register is not required. *Id.* at col. 6, lns. 9-11; col. 6, lns. 26-32; RX-2811C (Vojcic WS) at

Q&A 274-75. Claims 31 and 56 are directed to the "processing compensation factor" of the second method, [ ] *Id.*

iv. Funai

For those of Funai's products that interoperate with 802.11 standards devices and comprise at least one of Ralink's chips, this limitation is met by structure within Ralink's chips and inherently is met by structure within Funai's products. CX-1596C (Negus WS) at Q&A 414. For those Funai products that incorporate Realtek's chips, this claim limitation is not satisfied. *See* RX-2811C (Vojcic WS) at Q&A 274-75.

12. Claim 32

The record evidence shows that the accused products do not satisfy all limitations of claim 32. Dependent claim 32 recites, "[t]he receiver of claim 26, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal." It has been shown above that the accused products do not satisfy all limitations of claim 26 under the adopted claim constructions. Moreover, as discussed above with respect to claim 20, the timestamp does not account for delays in transmitting the signal. Therefore, the accused products do not satisfy this additional limitation of claim 32.

13. Claim 33

The record evidence shows that the accused products do not satisfy all limitations of claim 33. Dependent claim 33 recites, "[t]he receiver of claim 26, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol." It has been shown above that the accused products do not satisfy all limitations of claim 26 under the adopted claim constructions. Moreover, as discussed above with respect to claim 20, the timestamp does not

account for delays due to a busy signal. Therefore, the accused products do not satisfy this additional limitation of claim 33.

14. Claim 34

The record evidence shows that the accused products do not satisfy all limitations of claim 34.

a. A receiver, comprising:

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

b. a receiver counter that counts up to n counts, and

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

c. a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a traffic pending field and a timestamp field the traffic pending field including data indicating stations for which the transmitter has data buffered,

Claim 34 recites "a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a traffic pending field and a timestamp field the traffic pending field including data indicating stations for which the transmitter has data buffered." For an analysis of this claim limitation, refer to the corresponding discussions for claims 20 (radio modem) and 23 (traffic pending field).

d. the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer

Claim 34 recites "the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a

value m within a count sequence of the transmitter timer." For an analysis of this limitation, refer to the corresponding discussion for claim 20.

e. at the time of transmission of the transmission signal.

Claim 34 recites "at the time of transmission of the transmission signal." This claim limitation is construed to mean "at the beginning of the transmission of the packet." Complainants' proposed construction, which was not adopted, is "when the transmission signal is transmitted."

The record evidence shows that the accused Funai and Realtek products do not infringe this limitation under either construction, because [

] RX-2811C (Vojcic WS) at Q&A 257-59.

With respect to the Ralink chips, the evidence shows that [

] CX-1596C (Negus WS) at Q&A 423-27. Accordingly, it is determined that the Ralink chips, as well as the Funai products that incorporate these chips, satisfy this additional limitation of claim 34.

15. Claim 35

The record evidence shows that the accused products do not satisfy all limitations of claim 35.

a. The receiver of claim 34,

As shown above, the accused products do not satisfy all limitations of asserted claim 34 under the adopted claim constructions.

b. wherein the transmission signal further includes a timer interval field, and-the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending field.

The accused Funai and Realtek products do not satisfy this limitation because the '867 specification defines "timer interval field" as "the value of n of the modulo n counter in the transmitter," and the accused timer interval field is not that value. *See* JX-0005 ('867 patent) at col. 5, lns. 5-6; RX-2811C (Vojcic WS) at Q&A 277-81; RX-2813C (Heegard RWS) at Q&A 485-87, Q&A 511-12.

If, however, Complainants' proposed construction for the term '"timer interval field" were adopted, the record evidence demonstrates that the accused products would satisfy this claim limitation. The following section sets forth this evidence showing satisfaction of this limitation under the alternate claim construction.

i. 802.11 – Analysis Under Alternate Construction

As discussed above, the schedule period between Beacon frames is defined by "the dot11BeaconPeriod attribute within the AP." CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.1; CX-1596C (Negus WS) at Q&A 432. This defines a series of TBTTs, or "target beacon transmission times," "exactly dot11BeaconPeriod TUs apart." *Id.*; CX-0116C (802.11 Standard, Jun. 2007) at § 4. The TBTTs define the "timer interval" between periodic transmissions of transmission signals. CX-1596C (Negus WS) at Q&A 433.

The Beacon frame includes a field that indicates this scheduled time between Beacon frames. The "Beacon frame" ("transmission signal") specifically includes a "Beacon Interval field" which "represents the number of time units (TUs) between target beacon transmission times (TBTTs)." CX-0116C (802.11 Standard, Jun. 2007) at § 7.3.1.3; CX-1596C (Negus WS)

at 142, Q&A 434. Respondents' products [ ] CX-1596C (Negus WS) at Q&A 435; CX-0116C (802.11 Standard, Jun. 2007) at § 11.1.2.1 ("STAs shall adopt that beacon period when joining the BSS.").

ii. Doctrine of Equivalents

In addition to arguing literal infringement of this claim limitation under Complainants' proposed construction, Complainants also allege that the accused products satisfy this claim limitation under the doctrine of equivalents in the event Respondents' proposed construction is adopted. *See* Compls. Br. at 490-91. Complainants' doctrine of equivalents argument is not persuasive, however, because during prosecution the applicants told the USPTO that "the two counters 22 and 58 remain in synchronization as they cyclically count up to value n." RX-2811C (Vojcic WS) at Q&A 278-81; RDX-2811.0088; RX-1165 (file history of '661 application) at 80, 105, 132. The applicants surrendered timer interval fields that are not both the timer interval and the value of n of the modulo n counters in the receiver and transmitter.

The claimed and the accused "timer interval field" are also substantially different. RX-2811C (Vojcic WS) at Q&A 278-81. The function of the accused timer interval field [ ] but the claimed timer interval field provides both the interval and the maximum value of the count sequence in the counters in the receiver and transmitter timer so that the receiver knows the exact time to wake up. *Id.* at Q&A 279. The accused receiver [ ] but the claimed receiver knows the precise wake-up time, *i.e.*, n. *Id.* at Q&A 280. The result of the accused timer interval field [

] which is different from the claimed receiver, which wakes up precisely at time n to minimize power consumption. *Id.* at Q&A 281.

16. Claim 37

The record evidence shows that the accused products do not satisfy all limitations of claim 37. Dependent claim 37 recites, "[t]he receiver of claim 35, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal." It has been shown above that the accused products do not satisfy all limitations of claim 35 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 37, refer to the corresponding analysis with respect to claim 20.

17. Claim 38

The record evidence shows that the accused products do not satisfy all limitations of claim 38. Dependent claim 38 recites, "[t]he receiver of claim 35, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol." It has been shown above that the accused products do not satisfy all limitations of claim 35 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 38, refer to the corresponding analysis with respect to claim 20.

18. Claim 39

The record evidence shows that the accused products do not satisfy all limitations of claim 39. Dependent claim 39 recites, "[t]he receiver of claim 34, wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal." It has been shown above that the accused products do not satisfy all limitations of claim 34 under the adopted claim constructions. For a discussion

of the additional "timestamp" limitation of claim 39, refer to the corresponding analysis with respect to claim 20.

19. Claim 40

The record evidence shows that the accused products do not satisfy all limitations of claim 40. Dependent claim 40 recites, "[t]he receiver of claim 34, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol." It has been shown above that the accused products do not satisfy all limitations of claim 34 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 40, refer to the corresponding analysis with respect to claim 20.

20. Claim 47

Independent claim 47 includes all elements of independent claim 34 except the "traffic pending field" limitations. It has been shown above that the accused products do not satisfy the claim limitations of claim 34, notwithstanding the "traffic pending field" limitations of that claim. Therefore, for the same reasons discussed with respect to claim 34, the accused products do not satisfy all limitations of claim 47.

21. Claim 49

The record evidence shows that the accused products do not satisfy all limitations of claim 49.

a. A wireless local area network receiver, comprising:

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

b. a receiver timer that counts up to n counts, and

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

c. a radio modem capable of periodically receiving a transmission signal from a transmitter, the transmission signal including a timestamp

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

d. for synchronizing the receiver timer with a transmitter timer that counts up to n counts, the timestamp being a value m

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

e. which accounts for a delay between a start of a process to transmit the transmission signal from the transmitter and an actual time of transmitting the transmission signal,

For an analysis of this claim limitation, refer to the corresponding discussion for asserted claim 20.

f. wherein the receiver retrieves the timestamp and the receiver timer commences a count sequence based on the value m as to synchronize the receiver timer with the transmitter timer.

Claim 49 of the '867 patent recites, "the receiver timer commences a count sequence based on the value m," as distinguished from other claims that recite commencing a count sequence beginning at an "adjusted value," *e.g.*, claim 26. *See* RX-2811C (Vojcic WS) at Q&A 260. Thus, a person of ordinary skill would interpret the "receiver timer" in claim 49 to commence at "value m," and not an "adjusted value." *Id.* The accused timer in the accused products [ ] and thus does not satisfy this limitation of claim 49. *Id.*; RX-2813C (Heegard RWS) at Q&A 498, Q&A 505-06.

22. Claim 50

The record evidence shows that the accused products do not satisfy all limitations of claim 50. Dependent claim 50 recites, "[t]he receiver of claim 49, wherein the timestamp accounts for delays in a modem of the transmitter." It has been shown above that the accused products do not satisfy all limitations of claim 49 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 49, refer to the corresponding analysis with respect to claim 20.

23. Claim 51

The record evidence shows that the accused products do not satisfy all limitations of claim 51. Dependent claim 51 recites, "[t]he receiver of claim 49, wherein the timestamp accounts for delays due to a busy signal on a medium access protocol." It has been shown above that the accused products do not satisfy all limitations of claim 49 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 49, refer to the corresponding analysis with respect to claim 20.

24. Claim 52

The record evidence shows that the accused products do not satisfy all limitations of claim 52. Dependent claim 52 recites, "[t]he receiver of claim 49, wherein the receiver timer commences a synchronizing count sequence beginning at a value based on the timestamp." It has been shown above that the accused products do not satisfy all limitations of claim 49 under the adopted claim constructions. For a discussion of the additional limitation of claim 49, refer to the corresponding analysis with respect to claim 26.

25. Claim 53

The record evidence shows that the accused products do not satisfy all limitations of claim 53. Dependent claim 53 recites, "[t]he receiver of claim 52, further comprising circuitry for adjusting the value at which the count sequence begins." It has been shown above that the accused products do not satisfy all limitations of claim 52 under the adopted claim constructions. For a discussion of the additional limitation of claim 52, refer to the corresponding analysis with respect to claim 26.

26. Claim 54

The record evidence shows that the accused products do not satisfy all limitations of claim 54. Dependent claim 54 recites, "[t]he receiver of claim 53, further comprising an adder for adding a compensation factor to the value at which the count sequence begins." It has been shown above that the accused products do not satisfy all limitations of claim 53 under the adopted claim constructions. For a discussion of the additional "adder" limitation of claim 54, refer to the corresponding analysis with respect to claim 29.

27. Claim 55

The record evidence shows that the accused products do not satisfy all limitations of claim 55. Dependent claim 55 recites, "[t]he receiver of claim 54, wherein the compensation factor compensates for propagation delay at the receiver." It has been shown above that the accused products do not satisfy all limitations of claim 54 under the adopted claim constructions. For a discussion of the additional limitation of claim 55, refer to the corresponding analysis with respect to claim 30.

28. Claim 56

The record evidence shows that the accused products do not satisfy all limitations of claim 56. Dependent claim 56 recites, "[t]he receiver of claim 54, wherein the compensation factor allows for time taken to process the transmission signal at the receiver." It has been shown above that the accused products do not satisfy all limitations of claim 54 under the adopted claim constructions. For a discussion of the additional limitation of claim 56, refer to the corresponding analysis with respect to claim 31.

29. Claim 58

The record evidence shows that the accused products do not satisfy all limitations of claim 58. Dependent claim 58 recites, "[t]he receiver of claim 49, further comprising circuitry for commencing the synchronizing count sequence after the transmission signal is completely received." It has been shown above that the accused products do not satisfy all limitations of claim 49 under the adopted claim constructions. For a discussion of the additional limitation of claim 49, refer to the corresponding analysis with respect to claim 27.

30. Claim 59

The record evidence shows that the accused products do not satisfy all limitations of claim 59. Dependent claim 59 recites, "[t]he receiver of claim 58, further comprising circuitry for commencing the synchronizing count sequence after a CRC data in the received transmission signal is checked." It has been shown above that the accused products do not satisfy all limitations of claim 58 under the adopted claim constructions. For a discussion of the additional limitation of claim 59, refer to the corresponding analysis with respect to claim 28.

31. Claim 60

The record evidence shows that the accused products do not satisfy all limitations of claim 60. Dependent claim 60 recites, "[t]he receiver of claim 49, wherein the transmission signal further includes a traffic pending field that indicates stations for which the transmitter has data buffered." It has been shown above that the accused products do not satisfy all limitations of claim 49 under the adopted claim constructions. For a discussion of the additional limitation of claim 60, refer to the corresponding analysis with respect to claim 23.

32. Claim 61

The record evidence shows that the accused products do not satisfy all limitations of claim 61. Dependent claim 61 recites, "[t]he receiver of claim 60, wherein the transmission signal further includes a timer interval field, and the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending fields." It has been shown above that the accused products do not satisfy all limitations of claim 60 under the adopted claim constructions. For a discussion of the additional "timestamp" limitation of claim 61, refer to the corresponding analysis with respect to claim 35.

33. Funai / [ ] Products

In a separate section of their post-hearing brief, Complainants argue that Funai products that contain chips sourced from [ ] infringe the asserted claims of the '867 patent by virtue of their implementation of 802.11 functionality. *See* Compls. Br. at 595-96, 597. Complainants provide the following table that purports to list the Funai products accused of infringing the '867 patent that contain an [ ] chip, as well as relevant documentation showing 802.11 compatibility:

Product Number	Funai Model Number	WiFi Chip	Documentation Showing 802.11 Compatibility
[			CX-0994C ([1] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
			CX-0994C ([ ] Datasheet) at 1
		]	CX-0994C ([ ] Datasheet) at 1

Compls. Br. at 595-96.

With respect to these products, Complainants argue:

> The [ ] Chips claims compliance or interoperability with the IEEE 802.11b, 802.11g, or 802.11n standards. CX-0994C at 1. The datasheet for the [ ], which was products by [ ] in response to a subpoena in this investigation, clearly states that [
>
>]" *See*, for example, CX-0994C at 1, 30, 32, 35, 117. Products that claim compliance or compatibility with any of the IEEE 802.11 standards are, at minimum, more likely than not, and indeed highly likely, to infringe at least at least Claims 20, 23-24, 26-28, 32-35, 37-40, 47, 49-52, and 58-61 of the '867 Patent. CX-1643C (Negus Rebuttal Witness Statement) at 4, Q&A 11; 8, Q&A 42. Indeed, HDL code for numerous such products from Ralink and Realtek in this case demonstrates that the limitations of the asserted claims of the '867 Patent were met by all such products that claimed to have STA capability in

> compliance or interoperable with any of the IEEE 802.11 standards. *See* Section 6.B, *supra*.
>
> Accordingly, Funai Products that incorporate the [ ] Chip are highly likely to infringe Claims 20, 23-24, 26-28, 32-35, 37-40, 47, 49-52, and 58-61 of the '867 Patent. CX-1643C (Negus Rebuttal Witness Statement) at 4, Q&A 11; 8, Q&A 42.

Compls. Br. at 597.

Complainants have not adduced evidence to show that the Funai/[ ] products in question infringe the '867 patent. As an initial matter, the administrative law judge denied Complainant's motion to supplement the expert report of Dr. Negus to include infringement opinions related to the Funai/[ ] products. Order No. 84 (Mar. 28, 2013). The administrative law judge also granted Respondents' motion to strike portions of Dr. Negus' witness statement that opined on the alleged infringement of the Funai/[ ] products. Order No. 85, at 4 (Mar. 29, 2013). Accordingly, Complainants' infringement arguments are not supported by expert testimony.

Complainants instead generally allege, without evidentiary support, that these products are "more likely than not" and "highly likely" to infringe the asserted claims. *See* Compls. Br. at 597. Such a statement is not enough to prove that the Funai/[ ] products practice all elements of the asserted '867 claims. Therefore, it is determined that Complainants have not shown that the Funai/[ ] products infringe the asserted claims of the '867 patent.

D. Validity

1. Priority Date

The '867 patent matured from U.S. Patent Application No. 10/092,295 ("the '295 application"), which is a continuation of U.S. Patent Application No. 08/155,661 ("the '661 application"), which was filed on Nov. 22, 1993. The '867 Patent is entitled to a priority date of

no later than Mar. 6, 1993 based on Great Britain Patent Application No. 9304622 ("the '622 application"). *See* JX-0005.

Respondents argue that the '867 patent is not entitled to the claimed 1993 priority date because "the applicant allowed the '661 application to go abandoned before filing the '867 application." Resps. Br. at 136 (citing RX-1165 ('661 patent application) at RX-1165.0233). It is argued that "[t]he '867 patent would only be entitled to this earlier priority date if the '661 application was still pending (*i.e.*, not abandoned) when the '867 application was filed on March 7, 2002." *Id.* (citing 35 U.S.C. § 120).

Respondents' argument is not persuasive, however, inasmuch as the prosecution history of the '661 and '295 applications confirms that the '661 application was pending when the '295 application was filed. Respondents assert that the '661 application was abandoned on December 7, 2001, six months after a PTO rejection dated June 7, 2001. *See* Resps. Br. at 136. The record shows, however, that the PTO granted an extension of time to respond on December 7, 2001, and a Notice of Appeal was filed that same day. RX-1165 ('661 file history) at 224-225. The file wrapper contains another extension of time dated March 7, 2002, the day the '867 patent was filed. RX-1165 ('661 file history) at 227. The PTO issued a Notice of Abandonment over a year later on October 27, 2003. *Id.* at 233. The '295 application claimed priority to the '661 application and the '622 application from the outset. JX-0006 ('867 file history) at 37, 44. In its Notice of Allowability for the '867 patent, the PTO acknowledged the claim of foreign priority and indicated that certified copies of the required priority documents had been received. *Id.* at 187. Thus, the priority date of the asserted claims of the '867 patent is March 6, 1993.

2. Anticipation

The evidence adduced by Respondents has not shown, clearly and convincingly, that any prior art reference anticipates the asserted claims of the '867 patent.

a. European Patent No. 0615363 ("Diepstraten European Patent")

European Patent No. 0615363 to Diepstraten was published on September 14, 1994, and does not qualify as prior art to the '867 patent, inasmuch as it was determined above that the '867 patent is entitled to a priority date of March 6, 1993. *See* RX-0299 (EP 0615363B1). Therefore, the Diepstraten European Patent does not anticipate the asserted claims of the '867 patent.

b. Motorola WIN/White

Respondents argue that the system identified as "Motorola WIN/White" anticipates the asserted claims of the '867 patent.[57] Resps. Br. at 192-205. Motorola WIN/White is directed to a wireless in-building telecommunications system for voice and data communications using a TDMA protocol. CX-1641C (Katti RWS) at Q&A 494. Motorola WIN/White is a wireless packet TDMA system with a "plurality of time slots allocated for different users or purposes," and notes that synchronization is important so that a "receiving terminal" is "able to properly correlate the beginning of each frame," and that using a "timestamp" is known for such purposes. RX-0421 (White '482) at col. 1, lns. 55-62. Thus, Motorola WIN/White discloses a TDMA system, not a CSMA system. CX-1641C (Katti RWS) at Q&A 496.

One of the issues Motorola WIN/White addresses is the "need for an improved method for maintaining time synchronization in a wireless TDMA packet network in which multiple

[57] It is undisputed that Motorola WIN/White constitutes prior art to the asserted '867 claims. *See* CX-1641C (Katti RWS) at Q&A 485-547.

antennas are utilized" in order to solve synchronization problems specifically directed to "a wireless TDMA packet network in which different directional antennas are used for communications." RX-0421 (White '482) at col. 2, lns. 7-13. A person of ordinary skill in the art would understand TDMA to be a system where a central controller, called a "CM" in White, allocates access to the media on a repeating and deterministic basis for all of the terminals, each called a "UM" in Motorola WIN/White, in the network. CX-1641C (Katti RWS) at Q&A 498.

In the specific configuration of a directional antenna TDMA network disclosed in the Motorola WIN/White, each radio has 6 antennas so that communications between radios can occur in any one of 36 different combinations. RX-0421 (White '482) at Fig. 25, col. 16, lns. 52-63. Accordingly, the fundamental synchronization problem that Motorola WIN/White is addressing is stated as "[t]he use of different directional antennas complicates the problem of maintaining relative time synchronization between each of the UMs and the CM. RX-0421 (White '482) at col. 17, lns. 17-23. Since the UMs and CM each communicate using only one selected antenna at any given time, it cannot be assumed that each UM will receive synchronization signals or information transmitted by the CM using a particular CM antenna. CX-1641C (Katti RWS) at Q&A 499. The purported novelty of Motorola WIN/White is the use of "byte counters" in both the CM and UM wherein the value of the CM "byte counter" is transmitted at pre-determined "byte count" positions as a time stamp "TX_TIMESTAMP" in "frame sync packets" over antennas "A1, A3, and A5" for "odd" frame counts and antennas "A2, A4, and A6" on "even" frame counts. RX-0421 (White '482) at col. 17, lns. 31-52. The UM then attempts to receive on a particular UM antenna all "frame sync packets" from which the best choice of CM antenna for a particular UM at that time can be found and communicated back to the CM through techniques unrelated to synchronization, and timing synchronization of the

UM "byte counter" can be performed based partially on information in the "time stamp." CX-1641C (Katti RWS) at Q&A 502.

The positions in the CM "byte counter" for the time stamps can be determined in advance because this system is not subject to medium access delays. *Id.* at Q&A 503. Further, the TX_TIMESTAMP" is different from the timestamp in the '867 patent because it is not the value of the "byte counter" at the time of transmission of the time stamp. RX-0421 (White '482) at col. 18, lns. 3-18; CX-1641C (Katti RWS) at Q&A 504. Rather, the "TX_TIMESTAMP" represents the value in the byte counter relative to the start of the frame. *Id.* at Q&A 505.

The teachings of Motorola WIN/White are therefore in direct contrast with the teachings and asserted claims of the '867 patent. *Id.* at Q&A 508. Claim elements of the '867 patent that are missing from White include: (1) a timestamp that represents a value within a count sequence of a transmitter time at the time of transmission, (2) adjusting a timestamp and hence commencing a count at an adjusted timestamp, (3) using a compensation factor that allows for time taken to process the transmission signal, (4) a traffic pending field, (5) a timer interval field, and (6) accounting for delays due to a busy signal on a medium access protocol. *Id.* at Q&A 510.

Specifically with respect to the timestamp limitation, although Motorola WIN/White does show an operation to calculate a "compensation value OFFSET" that is used to restart the "UM frame byte counter," this operation is not an adjustment to the "retrieved timestamp" as claimed in the '867 patent. *Id.* at Q&A 511.

Motorola WIN/White does not disclose the limitation "timestamp field" as that term is used in all asserted claims of the '867 patent. *Id.* at Q&A 512. As discussed above, the "TX_TIMESTAMP" of White is not equivalent to the "timestamp field" of the '867 patent at

least because the "TX_TIMESTAMP" does not meet the limitation within the claim element of being a count value "at the time of the transmission." *Id.* In addition, this limitation is directed to the incorporation of the effects of delays in the transmitter and delays due to a busy signal on the medium. *Id.* Neither delay is accounted for by the TX_TIMESTAMP in White. *Id.* In fact, no such "busy signal" delays exist because Motorola WIN/White is a TDMA system. *Id.*

Motorola WIN/White does not disclose the claim element "the transmission signal including a timestamp field, the timestamp field including a timestamp having a value m for synchronizing the receiver counter with a transmitter timer, wherein the timestamp represents a value m within a count sequence of the transmitter timer [at the time of transmission of the transmission signal]" or similar limitations as used in the '867 patent. *Id.* at Q&A 519. As discussed above, the "TX_TIMESTAMP" referred to in White is not a "timestamp" within the meaning of the '867 patent because it is not the value of the "byte counter" at the time of transmission of the time stamp within the "frame sync packet." *Id.* The TX_TIMESTAMP "reflects a time X bytes after the start of the packet 1846 since Y bytes of buffering are utilized prior to the actual transmission of each byte, i.e. Y bytes are prefetched in preparation for transmission of each byte." RX-0421 (White '482) at col. 18, lns. 12-16; CX-1641C (Katti RWS) at Q&A 520-21. The TX_TIMESTAMP is an independent value reflecting a prefetched number of bytes and not the value of a counter in a transmitter timer. *Id.*

Motorola WIN/White does not disclose the claim element "wherein the timestamp accounts for delays due to a busy signal on a medium access protocol" as used in the '867 patent. *Id.* at Q&A 522. Motorola WIN/White discloses a TDD (Time Division Duplex) system, which is a variation on TDMA. *Id.* at Q&A 523. Such a system does not have a "busy signal on a medium access protocol." *Id.* As discussed above, the problem of a busy signal on a medium

access protocol is not a feature in TDMA systems because transmission times are predetermined. *Id.* Specifically, the positions of the CM "byte counter" in White for the time stamps can be determined in advance because this system is not subject to medium access delays. *Id.* Moreover Respondents' expert Dr. Heegard testified that the "busy signal" in the '867 patent is defined only in relation to CSMA systems and has no analogy in TDMA systems. Heegard Tr. 993-994, 996-997. Consistent with Dr. Heegard's testimony that the "busy signal" of the '867 patent does not appear in any TDMA system, there is nothing in the record demonstrating that the timestamp transmitted by the WIN system accounts for delays due to a "busy signal."

The evidence shows other important distinctions between the CSMA system of the '867 patent and the TDMA system of Motorola WIN/White as revealed by the testimony of Mr. Buchholz. In the Motorola WIN system, the device cannot sense whether the medium is "busy" and will send a request regardless of whether the medium is "busy" or not. Buchholz Tr. 935. The Motorola WIN system is thus fundamentally different from the CSMA framework of the '867 patent, and the concept of "busy signal" is absent. CX-1641C (Katti RWS) at Q&A 527.

This difference is significant because it confirms that the notion of a "delay" in accessing a medium is completely absent from Motorola WIN/White. *Id.* at Q&A 528. The CM in Motorola WIN/White never waits for the medium to be free before sending a signal. *Id.* Rather, it always sends a signal in its assigned timeslot. *Id.* If there is a collision and the CM is able to discern that there was a collision, it will send the signal again. *Id.* There is never a delay in accessing the medium, there is no busy signal, and thus there is no way for the alleged "timestamp" to account for such delays because there are no delays to account for. *Id.*

Motorola WIN/White does not disclose a "traffic pending field" as used in the '867 patent. *Id.* at Q&A 530. Mr. Buchholz's testimony confirms that no such disclosure appears in any document describing Motorola WIN/White. *Id.*; *see also* Buchholz Tr. 939.

Motorola WIN/White does not disclose the claim element "circuitry for adjusting a value, based on the timestamp, at which a count sequence begins at the receiver timer" as used in the '867 patent. CX-1641C (Katti RWS) at Q&A 533. Motorola WIN/White fails to disclose a timestamp in the context of the '867 patent and thus any limitation that includes "timestamp" is not disclosed in White. *Id.* White also specifically fails to disclose "adjusting" a timestamp as described above. *Id.*

Inasmuch as Motorola WIN/White fails to disclose a timestamp or circuitry for adjusting a timestamp, Motorola WIN/White also fails to disclose the following claim limitations which presume the presence of at least the "timestamp" limitation: "wherein the receiver counter commences a synchronizing count sequence at the adjusted value" or similar limitations as used in the '867 patent; "circuitry for commencing the synchronizing count sequence after the transmission signal is completely received" as used in the '867 patent; "circuitry for commencing the synchronizing count sequence after a CRC data in the received transmission signal is checked" as used in the '867 patent; "an adder for adding a compensation factor to the value at which the count sequence begins" or similar limitations as used in the '867 patent; "wherein the compensation factor compensates for propagation delay at the receiver" as used in the '867 patent; "wherein the compensation factor allows for time taken to process the transmission signal at the receiver" as used in the '867 patent; "wherein the receiver retrieves the timestamp" as used in the '867 patent; and "wherein the timestamp accounts for delays in a modem of the transmitter" as used in the '867 patent. *Id.* at Q&A 534-546.

Further, Motorola WIN/White does not disclose the claim element "wherein the timestamp accounts for a delay between a start of a process to transmit the transmission signal and an actual time of transmitting the transmission signal." *Id.* at Q&A 540. The "Y bytes" that Respondents identify as the delay are actually part of the signal transmission process. *Id.*; *see, e.g.*, Resps. Br. at 193-94. The Y bytes are predetermined because they are pre-fetched to buffer the packet. CX-1641C (Katti RWS) at Q&A 540. Thus, the "Y bytes" do not represent a "delay." There is no "delay" in the TDMA system of Motorola WIN/White as that term is used in the '867 patent. *Id.*

Finally, Motorola WIN/White does not discloses the claim element "wherein the transmission signal further includes a timer interval field, and the timer interval field includes timer interval data indicating an interval between periodic transmissions of transmission signals including traffic pending field." *Id.* at Q&A 542. Respondents have identified nothing in Motorola WIN/White that would meet this limitation. *Id.*

Therefore, it is determined that Respondents have not proved by clear and convincing evidence that Motorola WIN/White anticipates any asserted claim of the '867 patent.

c. U.S. Patent No. 5,052,029 ("James")

Respondents argue that U.S. Patent No. 5,052,029 to James (RX-1335) anticipates claims 20, 23, 24, 26, 29, 23, 33, 47, 49, 51, 52, 53, and 54 of the '867 patent. *See* Resps. Br. at 206-12; GR12 Filing at 21-22. It is undisputed that James is prior art to the '867 patent. *See* CX-1641C (Katti RWS) at Q&A 548-585.

James is directed to providing a synchronization signal for use on a wired communication interconnect. *Id.* at Q&A 554. In particular, James discloses a communication interconnect that connects multiple "units" such as "computers, peripheral devices, test equipment, or interfaces to

other types of equipment or communication interconnects." RX-1335 (James '029) at col. 2, lns. 40-44. The only specific "interconnect(s)" considered by James are wired media such as "printed circuit board trace, wire, coaxial cable, or optical media." *Id.* at col. 2, lns. 44-47.

The preferred embodiment in James is a "broadcast bus" that the "units" access through "bit-by-bit arbitration mechanism on a dominant-mode bus." *Id.* at col. 2, lns. 47-49; col. 3, lns. 18-20. "Bit-by-bit arbitration" in a wired system is fundamentally different from the type of communication disclosed in the '867 patent, in which devices communicate wirelessly and must wait for the medium to be free of busy signals. CX-1641C (Katti RWS) at Q&A 556. In contrast to the '867 patent, "bit-by-bit arbitration" involves the use of "arbitration bits" that are assigned to give certain "units" preferential bus access over other "units." *Id.*

In James, a "cycle master unit" is assigned an "arbitration number to insure it will obtain access to the interconnect" as soon as a fixed "long gap" of "absence of communications" by the "units" occurs following any already in progress bus activity at a "cycle synch point." RX-1335 (James '029) at Fig. 2, col. 3, lns. 41-54. The "cycle master unit" will always have access to the medium regardless of any other units after the "long gap" due to the "bit-by-bit arbitration." The cycle master unit's access to the medium is always deterministic and known in advance by the cycle master unit and other units. *See, e.g.*, *id.* at col. 13, lns. 29-36.

James is in direct contrast with the teachings and asserted claims of the '867 patent. *See* CX-1641C (Katti RWS) at Q&A 559. James does not disclose many of the asserted claim elements such as a timestamp field that represents a count sequence value at the time of transmission, adjusting a timestamp (and hence commencing a count at an adjusted timestamp), using a compensation factor for an adjustment, a radio modem, a traffic pending field, a timer interval field, or accounting for delays due to a busy signal on a medium access protocol. *Id.*