**UNITED STATES INTERNATIONAL TRADE COMMISSION**

**Washington, D.C.**

| **In the Matter of** | |
|---|---|
| **CERTAIN DEVICES CONTAINING NON-VOLATILE MEMORY AND PRODUCTS CONTAINING THE SAME** | **Inv. No. 337-TA-922** |

**ORDER NO. 10: CONSTRUING TERMS OF THE ASSERTED PATENTS**

(January 14, 2015)

The claim terms construed in this Order are done so for the purposes of this Investigation. Hereafter, discovery and briefing in this Investigation shall be governed by the construction of the claim terms in this Order. Those terms not in dispute need not be construed. *See Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1323 (Fed. Cir. 2004) (noting that the administrative law judge need only construe disputed claim terms) Any claim terms not discussed herein shall be deemed undisputed and shall be interpreted by the undersigned in accordance with "their ordinary meaning as viewed by one of ordinary skill in the art." *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1371 (Fed. Cir. 2003), cert. denied, 540 U.S. 1073 (2003).

# Table of Abbreviations

| | |
|---|---|
| CMIB | Complainant's Initial Markman Brief |
| CMRB | Complainant's Reply Markman Brief |
| CMSB | Complainant's Supplemental Markman Brief |
| RMIB | Respondents' Initial Markman Brief |
| RMRB | Respondents' Reply Markman Brief |
| RMSB | Respondents' Supplemental Markman Brief |
| SMIB | Staff's Initial Markman Brief |
| SMSB | Staff's Supplemental Markman Brief |
| Tr. | Transcript of the Markman Hearing |

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# I. INTRODUCTION

## A. Status

By publication of a notice in the Federal Register this investigation was instituted by the Commission on August 4, 2014. The International Trade Commission ordered that:

> Pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, an investigation be instituted to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain devices containing non-volatile memory and products containing the same by reason of infringement of one or more of claims 1, 2, 5, 7, 11, 12, 13, 17, and 27-29 of the '826 patent; claims 1, 2, 4, 5, 7, 8, 12, and 13 of the '757 patent; claims 1, 2, 7, 8, and 15 of the '324 patent; and claims 1-3 and 8-11 of the '330 patent, and whether an industry in the United States exists as required by subsection (a)(2) of section 337;

79 F.R. 45221 (August 4, 2014).

Pursuant to the Commission's notice, the Complainants in this Investigation are Macronix International Co. Ltd. and Macronix America, Inc. (collectively, "Macronix"). The named Respondents are Spansion Inc., Spansion LLC, Spansion (Thailand) Ltd., Aerohive Networks, Inc., Ciena Corporation, Delphi Automotive PLC, Delphi Automotive Systems, LLC, Polycom, Inc., Ruckus Wireless, Inc., ShoreTel Inc., Tellabs, Inc., Tellabs North America, Inc., and TiVo, Inc. (collectively, "Respondents").[1] The Office of Unfair Import Investigations is a party to this Investigation.

On November 18-19, 2014, a *Markman* hearing and tutorial was held in this Investigation, where the parties presented technology tutorials, (Tr. at 10-156), and participated in oral argument on several disputed claim terms. (Tr. at 6-315). Before the *Markman* hearing, the parties submitted several briefs setting forth their claim construction positions. Macronix and

[1] Macronix and Respondent Allied Telesis, Inc. ("Allied") jointly moved to terminate the Investigation as to Allied based on a Consent Order Stipulation, which I granted by Initial Determination on August 25, 2014. (Order No. 4).

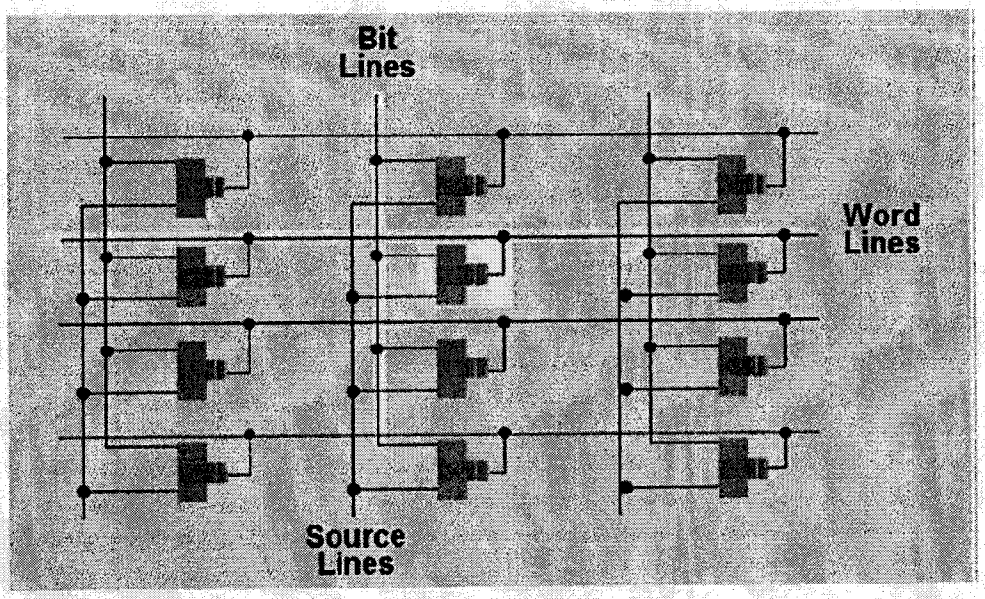
Respondents submitted their initial *Markman* briefs on October 21, 2014. The Staff submitted its *Markman* brief on October 28, 2013. Macronix and Respondents each filed reply *Markman* briefs on November 4, 2014. As requested during the *Markman* hearing (Tr. 160:19-163.1), Macronix, Respondents, and the Staff each submitted a supplemental *Markman* brief on December 5, 2015.[2]

### B. Technology Overview

The present investigation concerns four patents covering the structure and operation of certain non-volatile memory ("NVM"). As explained by Macronix, NVM is a form of memory that retains information even in the absence of a power source for extended periods of time. (CMIB at 1.) This means, as with "thumb drives" the devices will store data while apart from a powered device.

According to Macronix, NVM typically includes an array of memory cells arranged in rows and columns, where "bit lines" connect the cells in one direction, and "word lines" in the other. (*Id.*) In the example illustrated below of a memory cell structure, the bit lines connect to the drains of each column of memory cells, and word lines connect to the control gates of each row of memory cells. (*Id.*) When the proper signals are sent to a given bit line and word line (circuits not illustrated), the memory cell at the intersection of those two lines is read from or written to.

[2] The supplemental briefs only address the term "transmit[ing] the instruction, the address, or the read out data," which appears in claims 7 and 15 of Patent No. 8,341,324 and Respondent's position that I should find the claim to be indefinite.




(*Id.*)

In general, memory cells within a NVM device store information in the form of electrical charge. (*Id.*) Relevant to this Investigation are floating gates, where the memory cells are programmed by injecting electrons (the charge) into the cell by applying a high voltage. (*Id.*) Even after the voltage is removed, the floating gate retains the charge and can do so for long periods of time, even absent power. (CMIB at 1-2.) If a charge is determined to be stored on the floating gate, data can be read from memory. (*Id.* at 2.) A memory cell may be erased by removing the electrons and the typical convention is that an uncharged cell would be a "one" and a charged cell a "zero." (*Id.*)

Macronix alleges the patents at issue involve structural and operational improvements for non-volatile memory devices, *e.g.*, (1) Patent No. 5,998,826 is directed to a non-volatile memory cell structure and operational bias based on the use of a triple well floating gate memory cell that is suitable for use with low voltage power supplies; (2) Patent No. 6,031,757 is about a programmable write protection scheme providing flexibility and write protection features; (3) Patent No. 8,341,324 concentrates on a serial peripheral interface having improved data

transmission behavior; and (4) Patent No. 8,341,330 is about providing enhanced data read performance in an integrated circuit. (*Id.*)

## II. RELEVANT LAW

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*) (internal citations omitted), *aff'd*, 517 U.S. 370 (1996). Claim construction is a "matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *see also Markman*, 52 F.3d at 979. As the Federal Circuit in *Phillips* explained, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term" as understood by a person of ordinary skill in art at the time of the invention. 415 F.3d at 1313. "Such intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001).

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claims terms."

*Id.* at 1314; *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to 'particularly point [ ] out and distinctly claim [ ] the subject matter which the patentee regards as his invention."). The context in which a term is used in an asserted claim can be ""highly instructive." *Phillips*, 415 F.3d at 1314. Additionally, other claims in the same patent, asserted or unasserted, may also provide guidance as to the meaning of a claim term. *Id.*

The specification "is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term." *Id.* at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "[T]he specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs." *Id.* at 1316. "In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor." *Id.* As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323. In the end, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be ... the correct construction." *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)).

In addition to the claims and the specification, the prosecution history should be examined, if in evidence. *Id.* at 1317; *see also Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). The prosecution history can "often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Phillips*, 415 F.3d at 1317; *see also Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed.

Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

When the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence (*i.e.*, all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony, and learned treatises) may be considered. *Phillips*, 415 F.3d at 1317. Extrinsic evidence is generally viewed as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Id.* at 1317. "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

If, after a review of the intrinsic and extrinsic evidence, a claim term remains ambiguous, the claim should be construed so as to maintain its validity. *Phillips*, 415 F.3d at 1327. Claims, however, cannot be judicially rewritten in order to fulfill the axiom of preserving their validity. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999). Thus, "if the only claim construction that is consistent with the claim's language and the written description renders the claim invalid, then the axiom does not apply and the claim is simply invalid." *Id.*

## III. LEVEL OF ORDINARY SKILL IN THE ART

Neither Macronix nor Respondents took a written position of what qualifications a person of ordinary skill in the art (POSITA) would have in its filings.

The Staff opined that a POSITA with respect to U.S. Patent No. 5,998,826, (the '826 patent), is someone who had at least a bachelor's degree in electrical engineering or an equivalent degree, such as in material science or physics, and at least two years of experience in semiconductor process and fabrication technologies or semiconductor device and circuit design.

The Staff proposed that in the alternative, such a person would have had at least a master's degree in electrical engineering or an equivalent degree, such as in material science or physics, including study in the area of semiconductor process and fabrication technologies or semiconductor device and circuit design. (SMIB at 6-7.)

Concerning U.S. Patent No. 6,031,757 (the '757patent), the Staff opined that a POSITA is someone who had at least a bachelor's degree in electrical engineering, computer science, or physics, and at least two years of experience in designing or programming integrated circuit memory or digital interface circuits. (SMIB at 7.) With regard to U.S. Patent Nos. 8,341,324 and 8,341,330 (the '324 and '330 patents), the Staff posits that a POSITA is someone who had at least a bachelor's degree in electrical engineering, computer science, or physics, and at least one year of experience in digital hardware design. (*Id.*)

In consideration of the foregoing, I adopt the POSITA recommendations of the Staff.

## IV. THE '826 PATENT

### A. Overview

The '826 patent is titled "Triple Well Floating Gate Memory and Operating Method with Isolated Channel Program, Preprogram and Erase Processes." The USPTO issued the '826 patent on December 7, 1999 from U.S. Patent Application No. 08/817,656 ("the '656 application"), which was filed on April 4, 1997. The '656 application claims priority to Patent Application No. PCT/US96/14349, filed on September 5, 1996. The '826 patent has 32 claims, of which claims 1, 5, 12, 18, and 27 are independent. Macronix asserts Claims 1, 2, 5–7, 11–14, 17, and 27–29 of the '826 patent in this Investigation. *See* 79 Fed. Reg. 45221 (Aug. 4, 2014); Order No. 9, ID Granting Complainants' Motion for Leave to Amend Complaint and Notice of Investigation (Oct. 3, 2014) (unreviewed, Oct. 20, 2014). The '826 patent involves non-volatile memory cell

structure and operational bias based on the use of a triple well floating gate memory cell that is suitable for use with low voltage power supplies. (Complaint at ¶ 53.)

**B. Disputed Claim Terms**

**1. "extend[ing] substantially"**

The term "extend[ing] substantially" appears in claims 1, 11, and 17 of the '826 patent. The parties agree that "extending substantially" in claim 1 and "extend substantially" in claims 11 and 17 should be addressed together. (CMIB at 10 and RMIB at 16.) The parties propose the following constructions:

| Complainants | Respondents | Staff |
|---|---|---|
| No construction required (*i.e.*, "extend[ing] substantially") | "extend[ing] nearly across the channel(s)" | "extend[ing] across the channel and substantially" |

The term "extend[ing] substantially," is found in the relevant claims as follows:

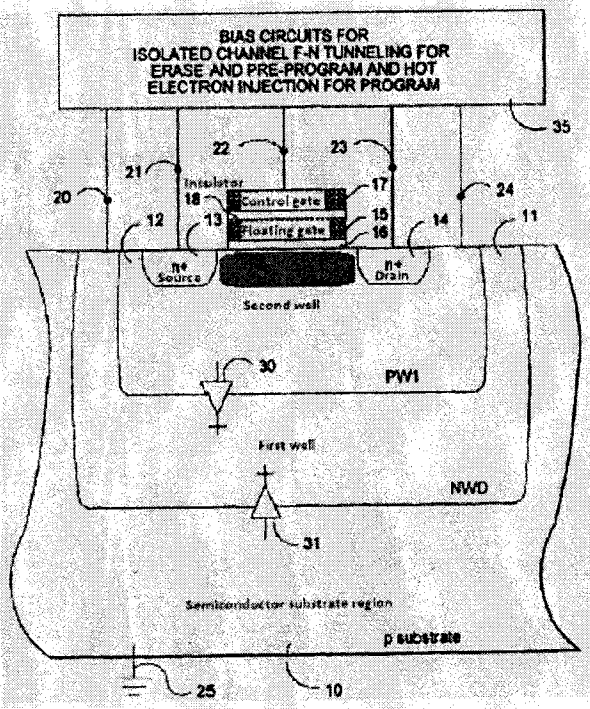
> Claim 1: "a floating gate structure disposed over the channel area and **extending substantially** from the source to the drain . . ."
>
> Claim 11: "wherein the floating gates of the array of floating gate memory cells are disposed over the respective channel areas and **extend substantially** between the respective sources and drains"
>
> Claim 17: "wherein the floating gates of the plurality of arrays of floating gate memory cells are disposed over the respective channel areas and **extend substantially** between the respective sources and drains"

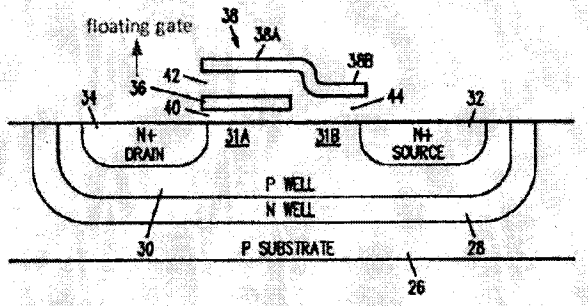
All parties agree the history of the patent during prosecution is relevant to constriction of this language. (*See* CMIB at 17-18; RMIB at 18-19; SMIB at 9.) Accordingly, I note that on May 6, 1998, the applicant amended application claim 11 (which became claim 1) and added application claims 41 and 42 (which became claims 11 and 17) in response to the Examiner's February 12, 1998 non-final rejection of all original claims under 35 U.S.C. § 103(a) based on U.S. Patent No. 5,341,342 ("Brahmbatt"). The applicant stated that "Brahmbatt expressly teaches away from a floating gate disposed over the channel area and extending substantially from the source to the drain . . . . Brahmbatt instead teaches a floating gate memory cell in which the

floating gate structure is ***disposed over only a portion of the channel area***[.]" (SMIB Exhibit 1 at MX-ITC-0000184 (emphasis added).) The Examiner rejected the applicant's arguments on May 29, 1998 and noted that while the applicant attempted to distinguish Brahmbatt by arguing that it provides for a floating gate "over only a portion of the channel area," the "Applicant's invention also extends over only a portion of the channel area[.]" (SMIB Exhibit 2 at MX-ITC-0000189.) On April 27, 1999, the applicant replied and distinguished Brahmbatt from the claimed invention as follows:

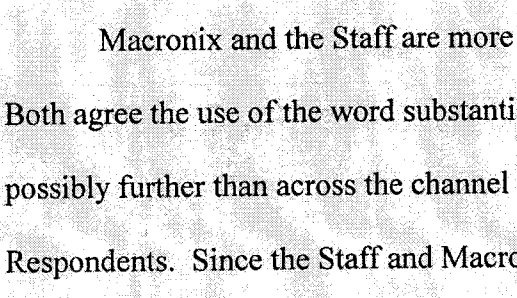
> The Brahmbatt reference describes a floating gate structure which does not extend across the channel from the source to the drain. Rather, Brahmbatt **intentionally includes a region over the channel which is not covered by the floating gate.** See column 3 lines 14–21 of Brahmbatt. This is a significantly different type of floating gate memory cell than that described and claimed in the present invention.

(SMIB Exhibit 3 at MX-0000237 (emphasis added).) Hence, the applicant argued that the floating gate of what became the '826 patent inherently differs from the floating gate of Brahmbatt because the floating gate of the '826 patent extends across the entire channel, whereas the Brahmbatt floating gate does not extend across the channel. *Id.* Illustrations follow:

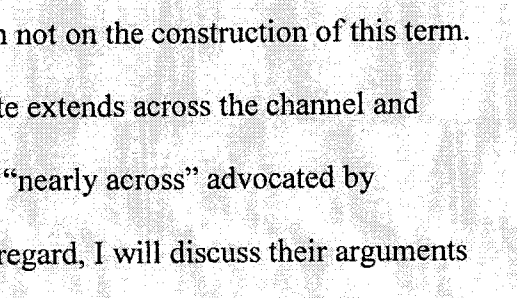


**'826 patent, Figure 1 (color annotations not in original)** (blue = channel area)



**Brahmbatt ('342 patent), Figure 3 (color annotations not in original)**



Macronix and the Staff are more in agreement than not on the construction of this term. Both agree the use of the word substantially means the gate extends across the channel and possibly further than across the channel as opposed to the "nearly across" advocated by Respondents. Since the Staff and Macronix agree in that regard, I will discuss their arguments concerning Respondents' proposed construction first.

The Staff and Macronix contend Respondents' proposed construction contradicts the applicant's intent and the prosecution history relating to this disputed term. (*See* CMIB at 16-17; SMIB at 11-12.) Respondents' proposed construction (the use of the word nearly) expressly allows the floating gate of the '826 patent to extend over only a portion of the channel. Nevertheless, this is precisely the attribute of the prior art Brahmbatt reference that the applicant used to distinguish the floating gate of the '826 patent. During prosecution, the applicant distinguished Brahmbatt based on the fact that it "instead teaches a floating gate memory cell in which the floating gate structure is *disposed over only a portion of the channel area*[.]" (*Id.*, at Exhibit 1 at MX-ITC-0000184 (emphasis added).) Despite this, Respondents propose the proper construction is the floating gate "extend nearly across the channel," allows for a gate that is "disposed over only a portion of the channel area." I find this construction to be incorrect based upon the word substantially and because Respondents' proffered construction is what the applicant disclaimed. Moreover, I note that Respondents' real concern here is that they not be found to infringe because Spansion's floating gate extends more than 100% over the channel. (Tr. at 29:6-30.14 and *see* Tr. at 32.) Thus, a reasonable conclusion is that Respondents' proposed construction is based upon preventing a finding of infringement and not upon the language in the

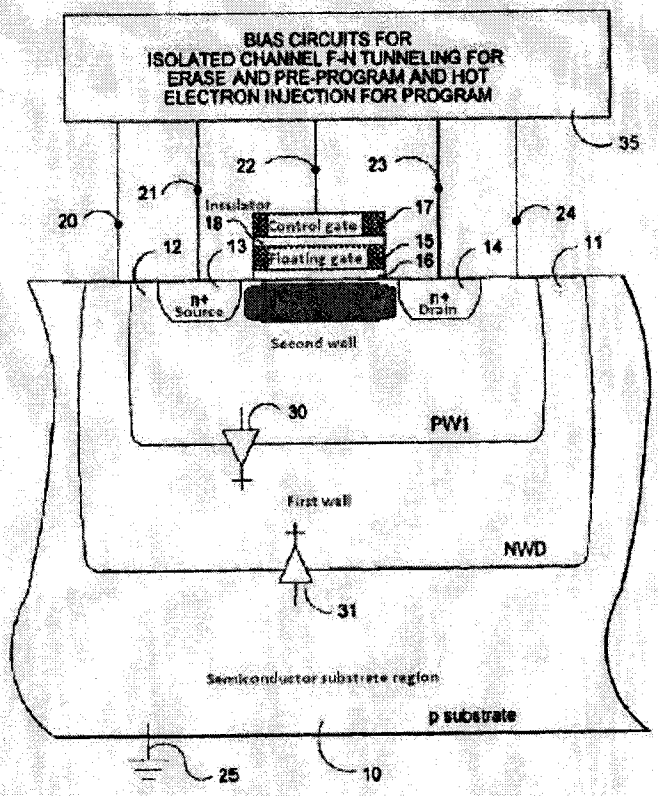
claim, the specification, or the patent history, a point that is buttressed by the discussion that follows.

I also note Respondents argued the floating gate cannot extend more than "substantially" from the source to the drain because they contend that Figure 3 from the Brahmbatt reference (reproduced with a single annotation, *supra*) reveals a floating gate that extends beyond the channel and over a portion of the drain. (RIMB at 20.) Respondents also seem to argue that Macronix, in order to overcome the Brahmbatt reference, amended the claims to add the words "extend[ing] substantially" to distinguish the claimed floating gate "disposed over the channel area" from the Brahmbatt floating gate that was disposed "over only a portion of the channel" and also over a portion of the drain. This is not persuasive.

Respondents' reliance on Figure 3 from the Brahmbatt reference for the proposition that it discloses a floating gate disposed over a portion of the drain is improper. Brahmbatt does not represent Figure 3 to be a scale drawing, nor does it purport to disclose any dimensions. Hence, Respondents' argument is entitled to little, if any, weight. *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000) ("[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.").

Even was I to agree, *arguendo*, that Figure 3 of the Brahmbatt reference is drawn to scale, Respondents' argument is still incorrect. Macronix clearly distinguished the floating gate of the Brahmbatt reference from the floating gate of the claims of the '826 patent when it asserted Brahmbatt extended over only a portion of the channel, while the present invention extends over the entire channel. I can find no language in the claims, the specifications, or the prosecution history requiring the floating gate terminate at the edge of the drain/channel or the source/channel junctions.

Instead, using Figure 1 from the '826 patent for illustrative purposes, if a floating gate were to extend from line **21** to line **23**, so that the floating gate were disposed over a portion of the source, the entire channel, and a portion of the drain, then, given the common understanding of the term, the floating gate would be understood as being disposed from or between the source to the drain.




A gate disposed over the entire channel, which is not depicted above, is distinguishable from a floating gate disclosed in Brahmbatt, because the former is disposed over the entire channel. Moreover, both the '826 patent and Brahmbatt do not say whether the floating gate can or cannot be disposed over any portion of the source or drain. Thus, I reject Respondents' arguments regarding the disposition of the claimed floating gate over the source or drain.

I note Respondents are concerned that "substantially" not mean the gate can extend more than 100% over the channel. (Tr. at 32; Tr. at 39:-40.) However, that is an insufficient reason to propose the indeterminate word "nearly" in place of another indeterminate word ("substantially")

in an effort to prevent infringement from being found. Such a substitution hardly solves the ambiguity Respondents allege exists. This is because the mere use of a synonym for "substantially" will not "address the ambiguity" of that word. *See C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004) (holding that "merely rephrasing or paraphrasing the plain language of a claim by substituting synonyms does not represent genuine claim construction"). Moreover, whether or not the word "substantially" applies to gates covering more than 100% of the channel is a proper question for a POSITA to address in evidence placed before me at a hearing. Even if the claims were broadened to the extent Respondents fear (more than 100% coverage), I find the substitution of the word "nearly" for the term "substantially" does not help.

As I stated during oral argument (Tr. at 35.), I did not understand the Staff's proposed construction. As explained by the Staff, if I adopted their proposed construction the language would read: "a floating gate structure disposed over the channel area and extending across the channel and substantially from the source to the drain." (Tr. at 35:20-25; Tr. at 38:22-24.) Essentially, I agreed with Macronix's argument that the Staff's proposed construction, adding the language "extending across the channel" is "unnecessary and potentially confusing." (CMIB at 10.)

Nevertheless, as the Staff accurately points out, Macronix agrees with the Staff's argument that the floating gate of the '826 patent must extend across the entire channel—"*i.e.*, does not leave a portion of the channel uncovered as Brahmbatt did." (CMIB at 19.) The Staff argues its proposed construction clarifies the claim language on this very point, which Macronix admits is a requirement for the claimed floating gate. (SMIB at 10.) Further, the exact language in claims 1, 11, and 17 recites a floating gate structure or floating gates that are "disposed" over the channel area and "extend[ing] substantially" between the source to the drain. According to the Staff, the

private parties incorrectly focus their construction only on the claim element requiring the floating gate to "extend substantially" between the source and drain, which could potentially allow for a floating gate that does not extend across the entire channel, a construction explicitly contrary to Macronix's own argument that the floating gate of the '826 patent must extend across the entire channel. (SMIB at 11.) Accordingly the Staff argues its construction should be adopted because it best incorporates the intent of the applicant as reflected in the prosecution history. (*Id.*)

In further support of its position, the Staff provided the language if changed to its proposed constructions (in bold) for the disputed claim term, to wit:

> Claim 1: "a floating gate structure disposed over the channel area and **extending across the channel and substantially** from the source to the drain . . ."
>
> Claim 11: "wherein the floating gates of the array of floating gate memory cells are disposed over the respective channel areas and **extend across the channel and substantially** between the respective sources and drains"
>
> Claim 17: "wherein the floating gates of the plurality of arrays of floating gate memory cells are disposed over the respective channel areas and **extend across the channel and substantially** between the respective sources and drains"

(*Id.*) The Staff argues these constructions are not potentially confusing and that they clarify the claim to reflect the intent of the applicant and the prosecution history. (*Id.*) Interestingly, the Staff says, when referring to the Complainants' proposed interpretation, that while not incorrect, I should not adopt it. (*Id.*) Instead, they argue I should adopt their construction.

I decline to accept the Staff's re-write of the claim language at issue. I find there is nothing significantly ambiguous about the term "extend[ing] substantially" within the context of claims 1, 11, or 17, especially in consideration of the Brahmbatt reference. Therefore, I give the language its plain and ordinary meaning. In so holding, I am not saying the word "substantially" is not capable of shades of meaning but that is the nature of the word. In these claims, "substantially" is the word the applicant chose and "substantially" is what the public is on notice of. In the instant situation this means the coverage can be less than 100% or more than 100%

coverage across the channel from the source[s] to the drain[s] as applied by a POSITA to the facts before him.

### 2. "the substrate is coupled to an external reference supply applying a ground potential and a positive supply potential"

This term appears in claims 1, 5, and 12 of the '826 patent. The parties have proposed the following constructions:

| Complainants | Respondents | Staff |
|---|---|---|
| "the substrate is coupled to an external voltage source configured to apply a ground potential and a positive supply potential" | indefinite | "the substrate is coupled to an external voltage source configured to apply a ground potential and a positive supply potential" |

Macronix and the Staff agree on a proposed construction for this disputed term. The Staff states their mutual proposed construction "hews closely to the claim language and reiterates the plain language of the term." (SMIB at 15.) However, the Respondents argue that the term is indefinite under 35 U.S.C. § 112, ¶ 2. (RMIB at 23.) Although I have independently construed the meaning of the language at issue as discussed below, it is important to understand that I cannot and will not accept Respondents' indefiniteness arguments at this juncture. First, they are improper because what Respondents are actually asking me to do is make a substantive ruling with a dispositive effect. In other words, Respondents should have moved for summary determination supported by statements from persons of ordinary skill in the art. Since the Commission has held that Markman Orders are not subject to review, I cannot accomplish what Respondents want. Despite Respondents' improper argument, I will address Respondents' argument insofar as it is relevant to me in construing the term at issue.

Respondents contend "[t]here is no way to tell which interpretation is correct" and that the term "is not precise enough to afford clear notice of what is claimed." (RMIB at 23–24.) Respondents argue that the term could be interpreted to mean either (i) that both a ground and a

positive supply potential are coupled to the substrate or (ii) that the substrate is coupled to an external reference supply that provides a ground and positive supply potential, but not necessarily applied to the substrate. On the other hand, both Macronix and the Staff contend a POSITA can readily understand the plain language of the term, especially in the context of the specification and the claims.

The disputed term appears in the preamble of claims 1, 5, and 12. In claims 1 and 5, the concepts of ground and positive supply potentials appear again in the last element of both claims:

> [voltage supply] circuits to induce [F-N] tunneling of electrons out of the floating gate[s] into the channel area[s] of the substrate by applying a positive voltage higher than the supply potential to the second well, a positive voltage to the first well, and a negative voltage to the control gate[s of selected cells], while the region of the substrate is grounded.

'826 patent, claims 1, 5 (the bracketed language is the additional language contained only in claim 5). Both the Staff and Macronix contend a POSITA reading the '826 patent would readily understand that the memory cells function by applying voltages between certain components or regions of the memory cell to create voltage gradients that cause electrons to flow the desired direction. (CMIB at 24-25; SMIB at 16; *see, e.g.*, Exhibit A ('826 patent) at 1:12–2:56.) Hence, depending on the conditions applied, a POSITA would readily understand that applying a positive supply potential is not necessary and can be contrary to effecting a functioning memory cell as claimed in the '826 patent. (SMIB at 16.)

Alternatively, Marcronix argues:

> As shown in the '826 patent specification, the external reference supply (or external "voltage source" under Macronix's and OUII's construction) is coupled to the semiconductor substrate of the memory cell and configured to apply both a ground potential and a positive supply potential. As clearly depicted below in the embodiment of Fig. 4 of the '826 patent, the substrate (which as the claim limitation language indicates, includes a region of p-type doping, the n-type and p-type wells, and the circuitry inside the box shown in the figure) is coupled to an external supply (not shown) that is configured to apply a ground potential (421) and a positive supply potential (422):

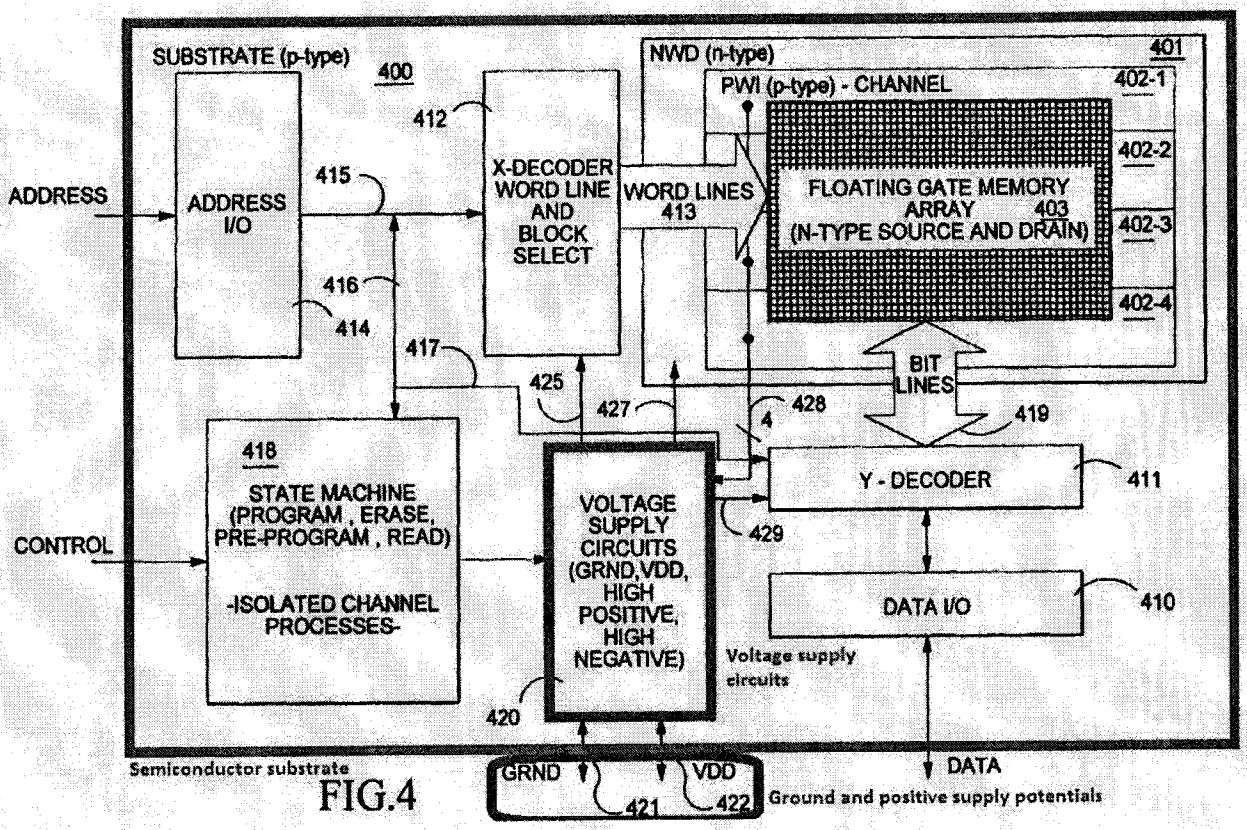



FIG.4

[Ex. A, Fig. 4 (annotated)]. This is a standard description of the application of power to an integrated circuit and would be readily understood by a person having ordinary skill in the art.

This claim language requires the ground potential and the positive supply potential be coupled to the semiconductor substrate, and the language of the specification supports this. [*See id.*, at 3:59-62 ("In one aspect of the invention, the substrate is coupled to an external reference supply that applies a ground potential and a positive supply potential."); *see also id.*, at 9:52-55 ("The substrate 400 also includes voltage supply circuits 420. The voltage supply circuits are coupled to an external ground on line 421 and to an external supply voltage VDD on line 422.")].

Further, a person having ordinary skill in the art at the time of the invention would have understood this claim language and been able to ascertain the scope of the claim. It would have been readily apparent to the skilled artisan that the external voltage source is configured to supply both a ground potential and a positive supply potential. [*See* Ex. D, at ¶18]. The skilled artisan would also have understood that the coupling between the semiconductor substrate and external voltage source includes components external to the semiconductor substrate that route the potentials to the semiconductor substrate. [*Id.*]. These external coupling components comprise, for example, VDD/GND pins and metal wires connecting the pins to in/out pads. [*Id.*].

Accordingly, this claim language is clear, unambiguous, and fully capable of being construed in view of the teachings in the specification. The construction proposed by Macronix and OUII closely tracks the claim language, and should be adopted.

(CMIB at 23-25;*see* Tr. at 47-51)

The Staff further asserts that if the disputed claim term were interpreted in the way Respondents suggest, *i.e.*, requiring both a ground and a positive supply potential to be coupled to the substrate, the final clause of claims 1 and 5 (*i.e.*, while the region of the substrate is ground) would become redundant and superfluous. (SMIB at 16.) The Staff asserts this is improper, for claim construction is not "an obligatory exercise in redundancy." *NTP, Inc. v. Research in Motion*, 418 F.3d 1281, 1311 (Fed. Cir. 2005), *cert. denied*, 546 U.S. 1157, 126 S.Ct. 1174 (2006). (*Id.*) According to both the Staff and Macronix, the '826 "patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, ___ U.S. ___, 134 S.Ct. 2010, 2129 (2014). (CMIB at 23; SMIC at 16.)

I agree with the construction advocated by the Staff and Macronix for the reasons stated by both. I note that during oral argument it became even clearer to me that Respondent's position is wrong. As succinctly emphasized by the Staff, a construction that renders the claimed invention inoperable should be viewed with extreme skepticism. (Tr. at 63.) Here, one of the interpretations offered by Respondents (the first one) creates an inoperable system and that makes no sense to me when the second alternative creates an operable system. This means, unlike Respondents argue (*See* RMIB at 24), the meaning proposed by Macronix and the Staff cannot be indefinite. This makes the source of both the ground potential and the positive supply an outside power source for the language at issue. (*See* Tr. at 66-67; 69-72.) Accordingly, I construe the language "the substrate is coupled to an external reference supply applying a ground potential and a positive supply potential" to mean: "the substrate is coupled to an external voltage source configured to apply a ground potential and a positive supply potential."

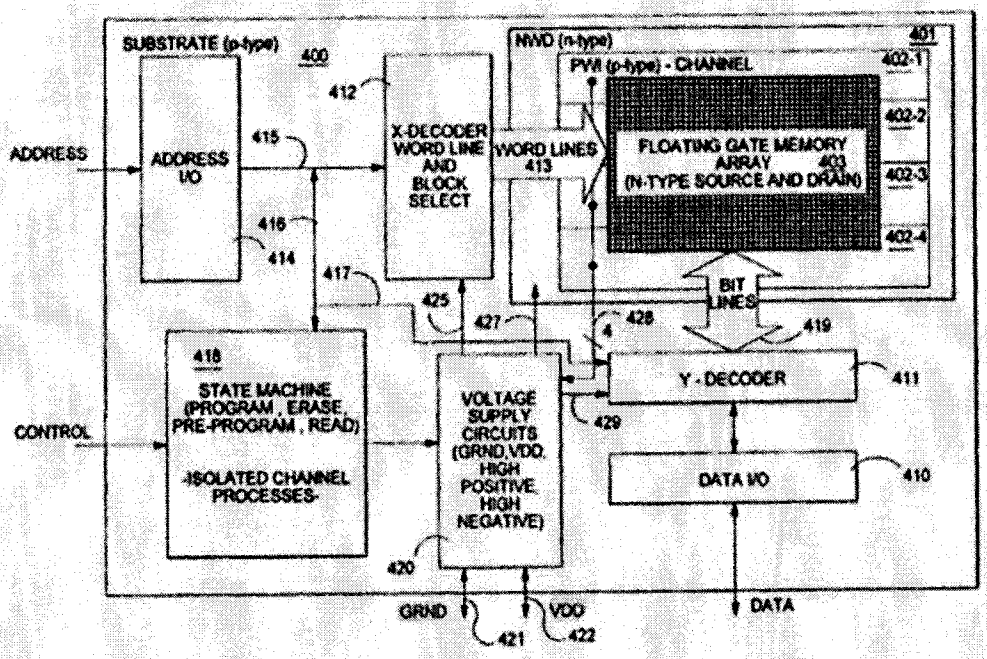
### 3. "the integrated circuit further including only a supply pin and a ground pin for supplying power to the integrated circuit"

Respondents identified "the integrated circuit further including only a supply pin and a ground pin for supplying power to the integrated circuit" as a term requiring construction. The term appears in claim 27 of the '826 patent. The parties have proposed the following constructions:

| Complainants | Respondents | Staff |
|---|---|---|
| ordinary meaning – OR– "the integrated circuit further including only a supply pin and a ground pin used to supply power to the integrated circuit" | "the integrated circuit that has a single supply pin and a single ground pin to supply power to the integrated circuit" | plain and ordinary meaning—*i.e.*, "the integrated circuit further including only a supply pin and a ground pin used to supply power to the integrated circuit" |

Originally (Joint Claim Construction Chart of October 14, 2014), the Staff agreed with the Respondents' proposed construction for this term. However, the Staff now believes the Complainants' proposed construction is more consistent with the intrinsic evidence and applicable case law and should be adopted.

Respondents claim Figure 4 and the description in the specification of the '826 patent supports their argument. (RMIB at 25.) Respondents' argue Figure 4 shows a "simplified block diagram of a flash memory integrated circuit ***according [to] the present invention***." (*Id.*) Respondents' point is that the invention is limited to Figure 4 because the invention is limited to Figure 4 as the present invention and argue *Edwards Lifesciences*, 582 F.3d 1322, 1329-31 (Fed. Cir. 2009) supports their argument. (*Id.*)




(RMIB at 26.) Respondents contend Elements 421 and 422 (outlined in yellow) of the invention represent the "external ground line" and "external supply voltage" line respectively. (*Id.*)

Continuing, Respondent argues:

> While the specification does not use the term "pin," the voltage supply circuits 420 are unquestionably coupled to the external ground on line 421 and to an external supply voltage VDD on line 422 through pins on the integrated circuit. *See id.* at Figure 4 and 9:53-55. The voltage supply circuits 420 are then used to supply ground and power to the circuits of Figure 4. *See id.* at 9:56-10:13. These are the only two pins disclosed or depicted in the figure that supply power to the integrated circuit. The descriptive portion of the specification also confirms this interpretation. In the "Summary of the Invention," the specification explains that "the present invention" is "suitable for use with ***a single*** low voltage power supply." *Id.* at 2:65-66. This single low voltage supply must be connected to the integrated circuit through a supply pin and a ground pin. There is no disclosure or suggestion that there are any embodiments within the scope of the claims that use multiple voltage power supplies, and therefore, more than two power supply pins (a ground pin and a supply pin).

(RMIB at 26-27.)

Respondent makes way too much of Figure 4. The specification describes Figure 4 as a "*simplified* block diagram of a flash memory integrated circuit according [to] the present invention." (emphasis added). While admitting that the specification does not use the term "pin"

in the context of discussing Figure 4, Respondents still rely on the fact that Figure 4 depicts "only two pins" that supply power to the integrated circuit in the figure. (*Id.*) Even if Figure 4 referred to pins, as a "simplified" diagram, there is no indication in the patent that the applicant intended Figure 4 of the '826 patent to limit "a" supply pin or "a" ground pin to "one" supply pin or "one" ground pin.

I am also persuaded by Macronix's logic that there is nothing in the claim that limits Claim 27 to only a single supply or ground pin. (Tr. at 83.) As counsel correctly points out, there is nothing that limits the power supply to one pin, which is a different concept than a singular power supply. Consequently, unlike Respondents contend (*See* Tr. at 87.) Figure 4 is merely a representation of power going into the circuit, not a representation of the number of pins. (Tr. at 84.)

Respondents also claim Complainants' proposed construction is ambiguous because it is susceptible to two different interpretations, *i.e.*, (i) the integrated circuit has a total of two pins or (ii) there are two pins to supply power to the integrated circuit, which has more than two pins total. (RMIB at 27.) Respondents are again wrong. My reading of the disputed term makes it clear that of all the pins included on the integrated circuit, only the supply and ground pins supply power to the integrated circuit. This is the only possible grammatically correct and reasonable interpretation in light of the case law regarding the meaning of the article "a." Specifically, the CAFC has consistently held that: "As a general rule, the words 'a' or 'an' in a patent claim carry the meaning of 'one or more.'" *TiVo, Inc. v. EchoStar Commc'ns Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008); *see also KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) ("This court has repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'"); *SanDisk Corp. v. Kingston Tech. Co., Inc.*, 695 F.3d 1348, 1360–61 (Fed.

Cir. 2012) (concluding that "a" means "one or more"). "The exceptions to this rule are extremely limited: a patentee must evince[] a clear intent to limit 'a' or 'an' to 'one.'" *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008), *citing KCJ*, 223 F.3d at 1356. Given this well understood precedent and the claim and specification language before me, it would be clear error for me to construe the disputed term in such a way to limited it to a single supply pin and a single ground pin.

Based upon the foregoing and the clear language of the disputed language itself, I find the instant term shall be given its plain and ordinary meaning, that is the term "the integrated circuit further including only a supply pin and a ground pin for supplying power to the integrated circuit" means what it says.

## V. THE '757 PATENT

### A. Overview

The '757 patent is titled "Write Protected, Non-volatile Memory Device with User Programmable Sector Lock Capability." The USPTO issued the '757 patent on February 29, 2000 from U.S. Patent Application No. 08/825,879 ("the '879 application"), which was filed on April 2, 1997. The '879 application claims priority to Patent Application No. PCT/US96/18674, filed on filed on November 22, 1996. The '757 patent has 33 claims, of which, Claims 1, 15, and 25 are the independent claims. Macronix asserts claims 1, 2, 4, 5, 7, 8, 12, and 13 of the '757 patent in this Investigation. *See* 79 Fed. Reg. 45221.

### B. Disputed Claim Terms

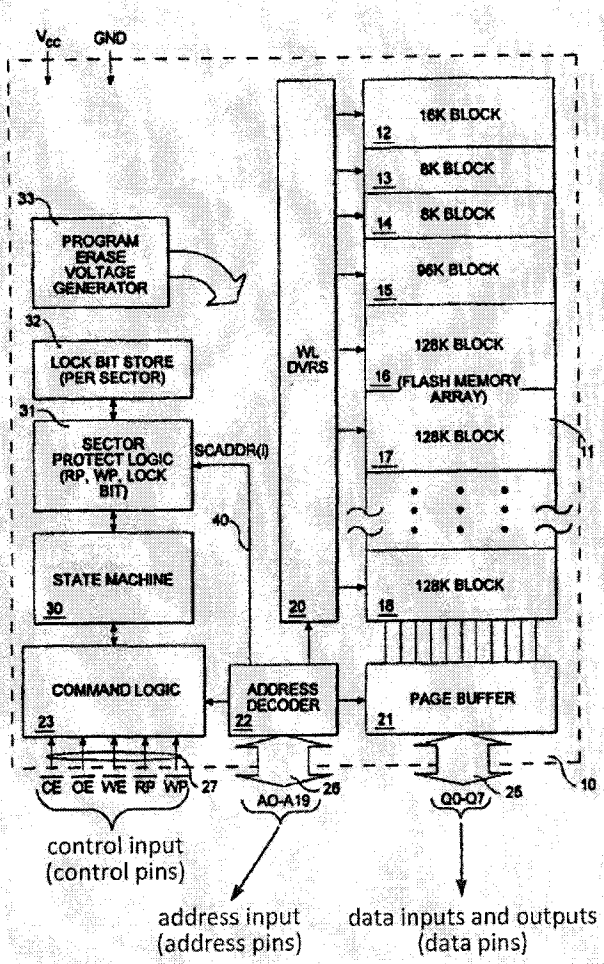
#### 1. "control inputs", "address inputs", and "data input/outputs"

Respondents identified "control inputs," "address inputs," and "data input/outputs" as terms that require construction. Complainants also identified "control input" as terms requiring construction. The term "control input(s)" appears in claim 1 of the '757 patent and the terms

"address inputs" and "data input/outputs" appear in claims 1, 4, and 13 of the '757 patent. The parties agree that the central dispute to all three terms is whether or not the pins are "dedicated,"*i.e.*, are the pins limited to only the single specified function. The parties propose the following constructions:

| | Complainants | Respondents | Staff |
|---|---|---|---|
| control inputs | "pins on an integrated circuit for receiving control signals" | "dedicated control pins" | plain and ordinary meaning—*i.e.*, "pins on an integrated circuit for receiving control signals" |
| address inputs | ordinary meaning – OR – "pins on an integrated circuit for receiving address signals" | "dedicated address pins" | plain and ordinary meaning—*i.e.*, "pins on an integrated circuit for receiving address signals" |
| data input/ outputs | ordinary meaning – OR – "pins on an integrated circuit for transferring data into or out of a memory array" | "dedicated input/output pins" | plain and ordinary meaning—*i.e.*, "pins on an integrated circuit for transferring data into or out of a memory array" |

In at least one preferred embodiment, the '757 patent discloses that an address decoder is coupled to a set of address inputs and command logic is coupled to a set of control inputs. ('757 patent at 5:29–32; *see* 7:42-44, 3:9-11.) Respondents argue the specification references support their contention that the disputed terms perform only a single dedicated function. (RMIB at 31-32.) Respondents argue there is no disclosure or suggestion the claimed inputs can perform more than one distinct function. (RMIB at 31.) Continuing, Respondents argue that Figure 1 of the '757 patent supports their argument by illustrating the three distinct claimed groups of pins for (1) control, (2) address, and (3) data input/output, to wit:




(*Id.*, annotations in red by Respondent.) Respondents argue the following text, consistent with Figure 1 proves its point, e.g.,

> "***[a]ddress inputs*** receive ***address signals***, and ***data input/outputs*** (I/Os) provide a path for ***transferring data into and out of the array*** on the integrated circuit." *Id.* at 3:9-11; *see also, id.* at 3:7-9 ("A plurality of ***control inputs*** is provided on the integrated circuit ***for receiving a set of control signals***"); 5:28-32 ("Page buffer 21 is connected to a set of **data I/O pins**, generally 25, designated Q0-Q7. Address decoder 22 is coupled to a set of **address inputs** 26, designated A0-A19. Command logic 23 is coupled to a set of **control inputs** 27 which receive a corresponding set of control signals.").

(RMIB at 32, bold text by Respondents.) Respondents also contend the peripheral interface architecture contemplated by the inventors of the '757 patent, known as parallel architecture, which necessarily uses a large number of dedicated pins to transmit control and address signals

and data in parallel, would have to be changed significantly if the pins were multi-purpose. (*Id.*) Closing out this thought, Respondents argue the patent lacks any disclosure that would inform a POSITA that the inventors knew a way to "reconstruct the claimed integrated circuits to work properly without using dedicated pins." (*Id.*)

The Staff and Macronix disagree and argue Respondents are relying upon excerpts from the specifications that arise from a single preferred embodiment and that Respondents advocate an overly narrow construction of the claims and that is contrary to the disclosed embodiments of non-dedicated control/address/data pins in the ''757 patent. (CMIB at 33-34 and SMIB at 19-21.) The Staff notes the Federal Circuit has cautioned that particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Phillips*, 415 F.3d at 1323; *Kara Tech. Inc. v. Stamps.com Inc.*, 582 F.3d 1341, 1348 (Fed. Cir. 2009) ("The patentee is entitled to the full scope of his claims, and we will not limit him to his preferred embodiment or import a limitation from the specification into the claims."). (SMIB at 19-20.)

In reviewing Respondents' argument, I note the specification does clearly disclose that in another aspect of the invention, command logic is coupled not only to the control inputs, but to the address inputs and data input/outputs as well, allowing the address inputs and data input/outputs coupled to the command logic to detect command sequences. (3:11–15.) This text provides:

> Command logic is coupled to the plurality of control inputs, and to at least one of the address inputs and data I/Os, and *detects command sequences at the plurality of control inputs and at least one of the* address inputs *and the data I/Os*.

(emphasis added) This text clearly explains that address inputs may perform multiple functions. It is fair to say this text discredits Respondents' argument, because it teaches that at least the address input and the data input/outputs are not dedicated pins that are functionally segregated by their nomenclature.

Perhaps anticipating the fatal weakness I have just noted, Respondents also argue that not requiring these disputed terms to be "dedicated pins" improperly broadens the scope of the claims and introduces redundancy. (RMIB at 33.) Respondents contend the modifiers "control," "address," and "data" in the text of the claims are being read out by the Staff and Macronix to become mere pins that are indistinguishable from one another. (*Id.*) Respondents illustrate their point as follows:

| Actual Claim Language | Macronix's Construction |
|---|---|
| control inputs for receiving a set of control signals | pins on an integrated circuit for receiving control signals |
| address inputs for receiving address signals; | pins on an integrated circuit for receiving address signals |
| data input/outputs for transferring data into and out of the array; | pins on an integrated circuit for transferring data into or out of a memory array |

(*Id.*) According to Respondents, by comparing the language that does not overlap, it can be seen that Macronix (and the Staff) are construing the term "inputs" as "pins on an integrated circuit" and reading out the descriptive modifiers of each claim term. (RMIB at 34.)

Concerning the Respondents' redundancy argument, I note the Staff concedes its construction, if substituted into claim 1 in place of the disputed terms, is somewhat redundant. (SMIB at 20.) Specifically, Claim 1 provides:

> An integrated circuit memory, comprising:
>
> . . .
>
> a plurality of control inputs [pins on an integrated circuit for receiving control signals] for receiving a set of control signals;
> address inputs [pins on an integrated circuit for receiving address signals] for receiving address signals;
> data input/outputs [pins on an integrated circuit for transferring data into or out of a memory array] for transferring data into and out of the array;
>
> . . . .